Arrow and Texas Instruments
JESD204B Hardware Lab Tutorial

Version 14.0 **09/29/2014** **Tutorial**

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OVERVIEW

The **Altera SoC** combines a **Hard Processing System** (HPS) and an **FPGA** on a **single device**. The HPS has dual core **ARM Cortex-A9 MPUs** and a host of peripherals such as DDR3 controllers, Ethernet MACs, SPI controllers and many more. The FPGA portion of the device is tightly coupled through **high performance bridges** to the HPS. The designer can add peripherals they create or from third party IP to the FPGA and map it into the HPS. **Thus you have a flexible and very powerful solution**.

JEDEC JESD204 is an industry standard that was specifically designed to facilitate the interconnection of D/A and A/D converters to digital ICs in general, and FPGAs in particular. The first revision, the JESD204 2006 specification, brought the advantages of SERDES-based high-speed serial interfaces to data converters, but it supported only a single lane with a single link with a maximum bandwidth of 3.125 Gbps.

In 2008, the second revision of the standard was released, JESD204A, which added support for multiple data lanes and also lane synchronization. Lane synchronization enables JESD204A to be used in quadrature (I/Q) sampling systems, where this technology underpins modern 3G, 3G+, and 4G broadband wireless communications.

In 2011, a third revision of the specification, JESD204B [JESD204B.01], has been published. JESD204B supports 8B/10B encoding, pre-emphasis, and equalization. JESD204B also introduces new enhancements, including a higher maximum lane rate (higher bandwidth), support for deterministic latency, and support for harmonic frame clocking.
The MTI IPC-JESD204-B controller in its receiver and transmitter modules is implemented in RTL VHDL-93 language according to the JEDEC JESD204B.01 standard. The implementation is suited for FPGAs, ASSPs and ASICs in a number of different technology processes.
Designs employing JESD204 enjoy the benefits of a faster interface to keep pace with the faster sampling rates of converters. In addition, there is a reduction in pin count which leads to smaller package sizes and a lower number of trace routes that makes board designs much easier and offers lower overall system cost. The standard is also easily scalable so it can be adapted to meet future needs.

MTI's IPC-JESD204-B offers the following competitive advantages:

- Support of rates up to 12.5 Gbps (depends upon the family and speed grade of the device)
- 32-bit internal data processing with clock frequency 1/40 of baud rate in use enable usage in low end and mid end FPGAs
- MCDA-ML (Multiple-Converter Device Alignment, Multiple-Lanes)
  - Disabling of features mandatory to a class MCDA-ML module, if connected to a device pertaining to a class that does not support these features (JESD204 standard).
- Support for run-time programmable configuration for key parameters
  - L, M, F, N, HD, SCR, CS
  - Support for deterministic latency (subclass 1)
  - Support for backward compatibility to JESD204A (subclass 0)
  - Insertion of tail bits are performed based on register settings. Both constant and low DC content tail bits are supported.
  - Support for built in test modes
- Support for error handling
- Includes 8b10b coding block
- Separate CPU interface for control and monitoring

This lab provides an interface to the ADC34J22 via the JESD204B IP core from MTI so that a hardware developer will have:

A complete customized Hard Processor System (HPS) SoC system to interface to the ADC34J22

An HPS in Qsys to realize a custom ARM SoC system with bridges to the FPGA/ADC34J22

A reference on how to use System Console to verify the ADC34J22

The HPS is **configured** using **Qsys**, Altera's SoC/FPGA IP integration tool. Configuration includes **selecting DDR memory**, determining **clock frequencies** and selecting which **HPS peripherals** your design will use. As such, Qsys provides the system architecture to interface to the **ADC34J22**. In this example, Qsys is used to define the **HPS peripheral pin outs and** Quartus is used to define the **FPGA peripheral pin outs** to the HSMC interface, which includes the ADC34J22.

MODULE 1. Getting Started

Your first objective is to ensure that you have all of the items needed and to install the tools so that you are ready to create and run your design.

List of Required Items:

- Arrow Electronics **SoCKit** development board
- **Quartus II** v14.0 Web Edition
- Computer with Windows 7, a minimum of 4 GB RAM, a minimum of I3 core and over 10 GB free hard disk space for the Quartus II install
- **Lab Design Files**
- **DEV-ADC34J22 Evaluation Module**

1.1 Acquiring Cyclone V SoCKit

To order a SoCKit please click on the link below

Order a SoCKit from Arrow Electronics

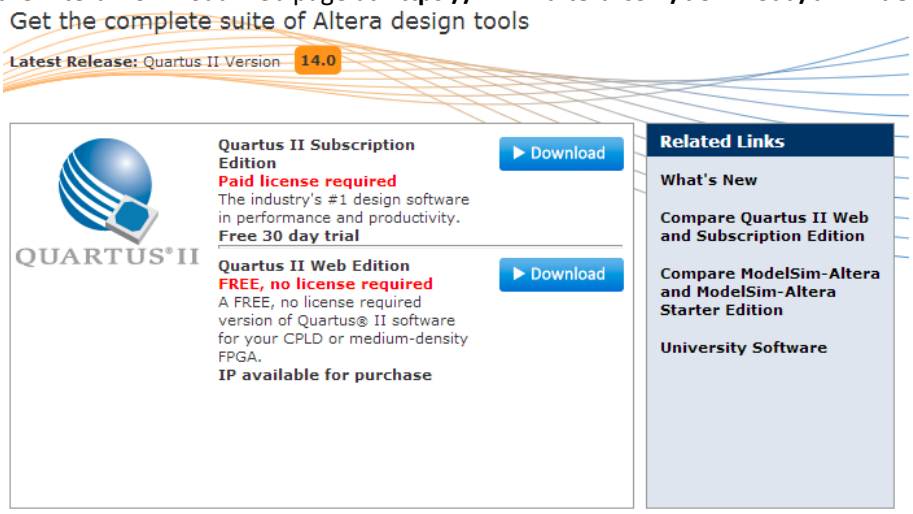
1.2 Install the Altera Design Software

You will need to install the following design software package:

- **Quartus II Web Edition design software v14.0.** – FPGA synthesis and compilation tool that contains Qsys and the MegaCore IP library with the SoC processor

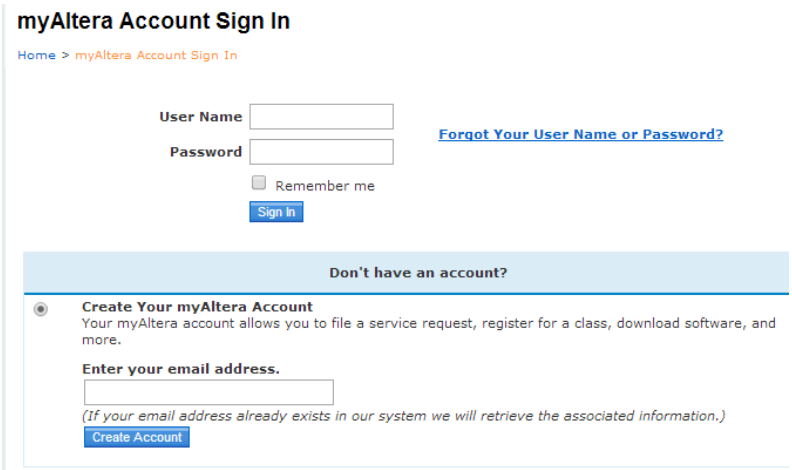
The following steps will guide you through the installation instructions. Quartus II Web Edition can be downloaded from the Altera web site. ***Please carefully follow the steps shown below***.

- Go to the Altera Download web page at **https://www.altera.com/download/dnl-index.jsp**

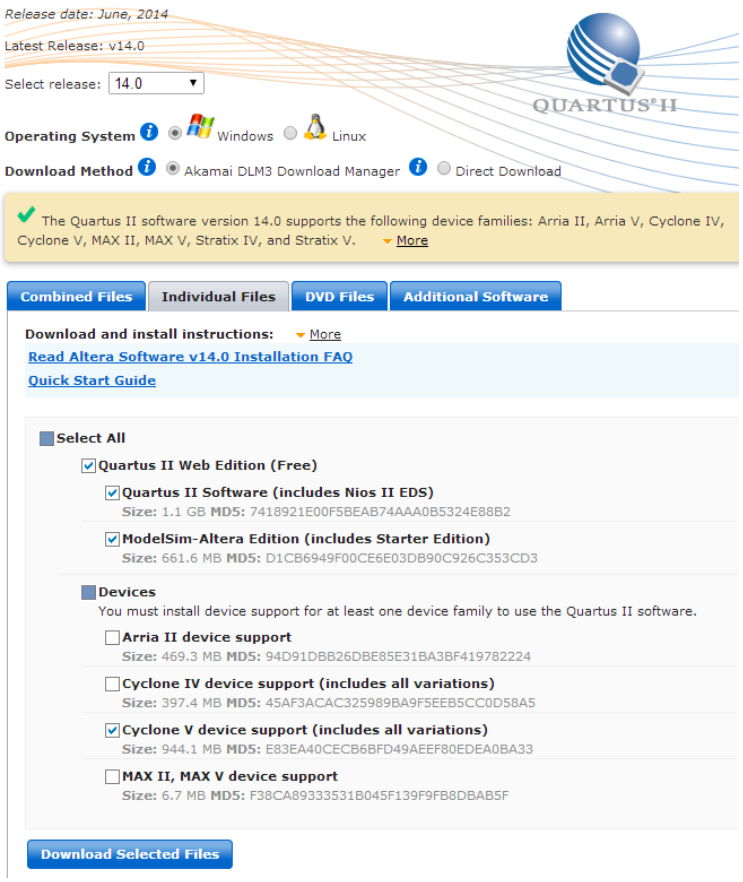


- Select "**Quartus II Web Package 14.0.** Press the **Free Web Package** button.

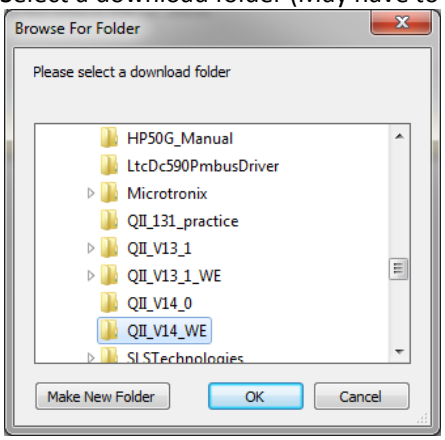
- Login to **myAltera** account. Use your **existing login**, or **Create Your myAltera account.**



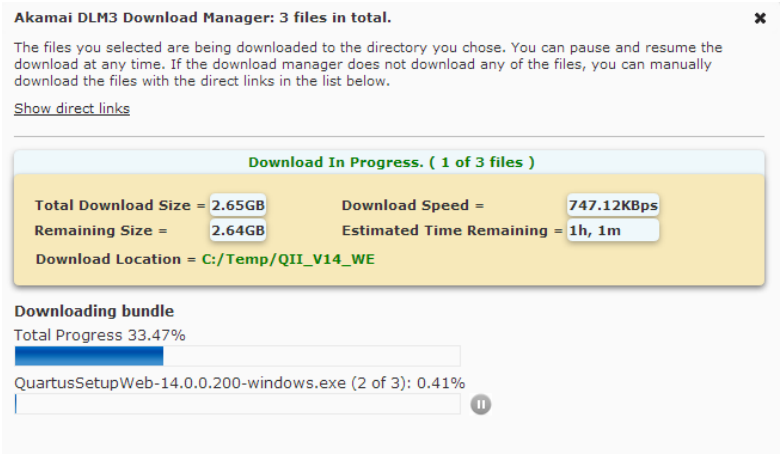
- Select **Quartus II Web Edition, Windows**:
- **Select the "Individual Files" Tab**
- **Select the " Download Selected Files" Button**
- **Download** the Quartus II software files onto your computer.



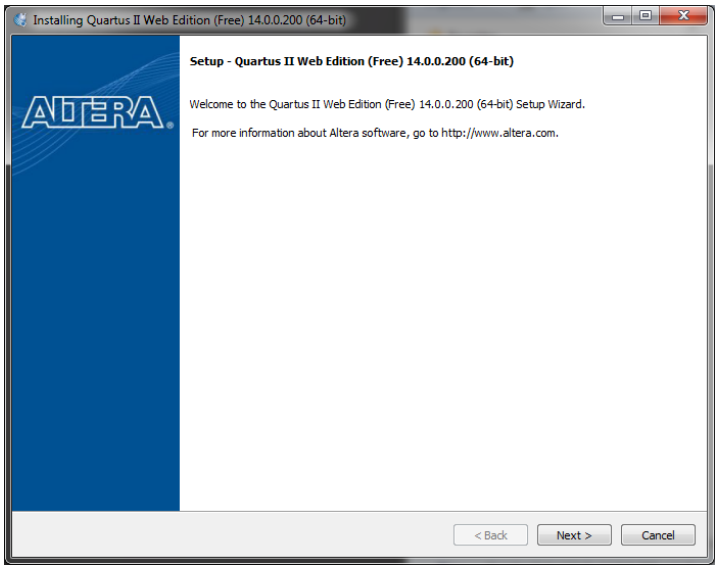
- Select a download folder (May have to Make New Folder)



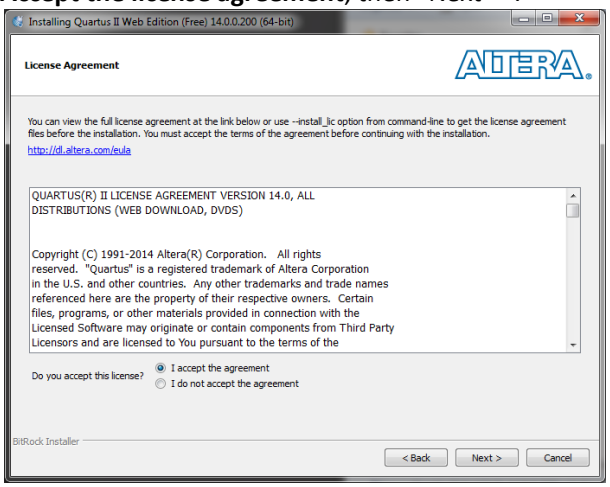
- The files will then be downloaded via the Download Manager



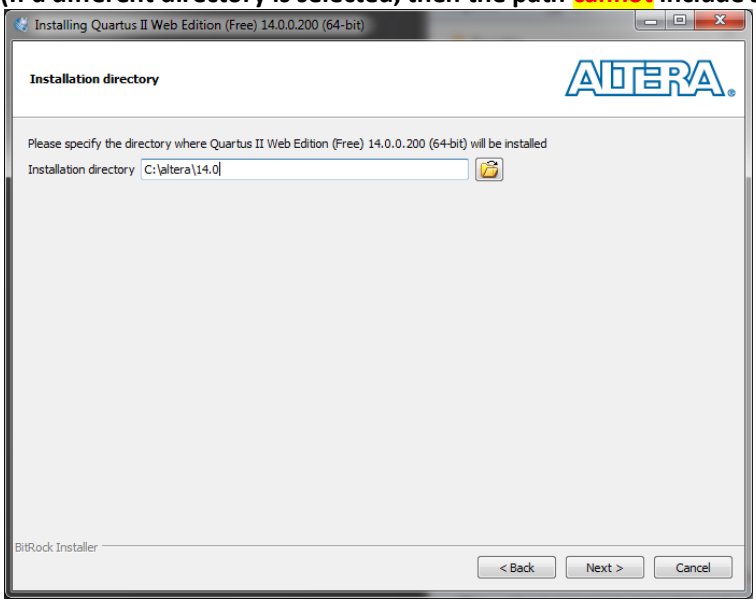
- After the **file** is downloaded on the computer, select the *.exe file, and **install the software**.



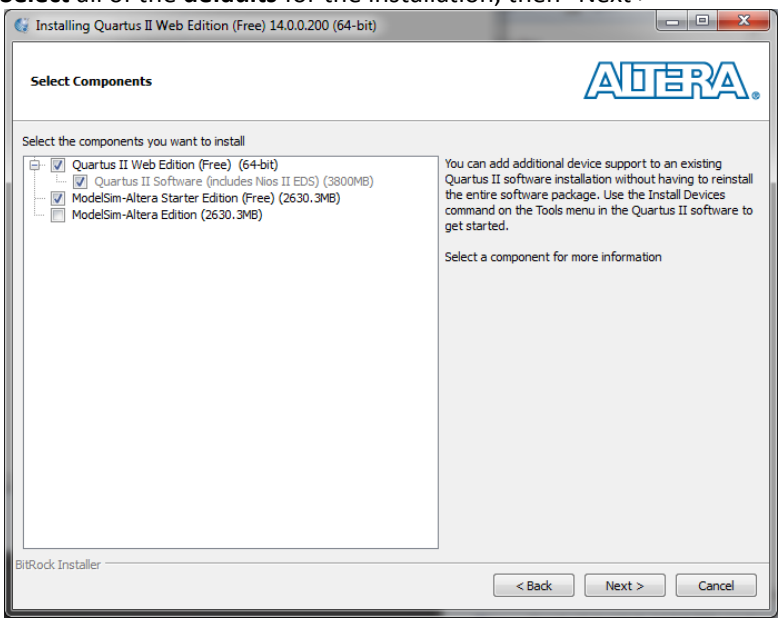
- **Accept the license agreement**, then “Next >”.



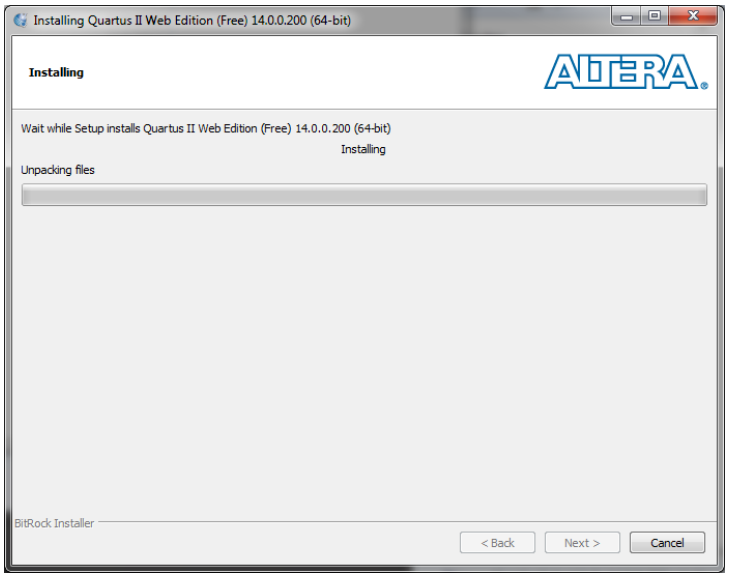
- **Select** the **default** installation directory, then “Next >”
  (If a different directory is selected, then the path cannot include spaces).



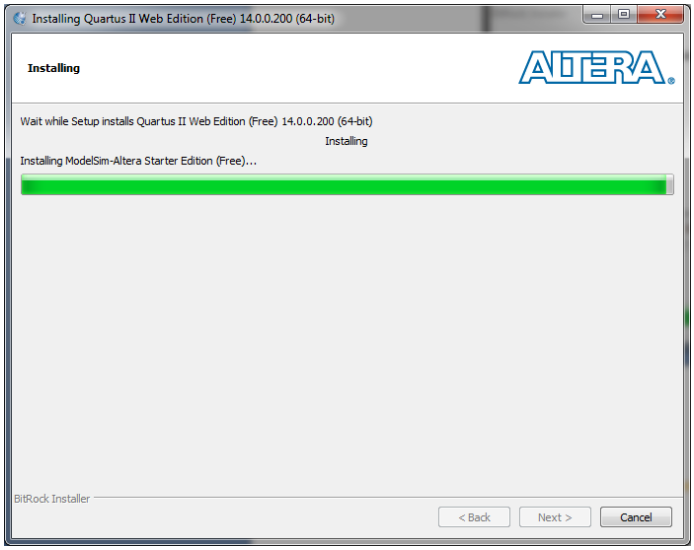
- **Select** all of the **defaults** for the installation, then “Next >”

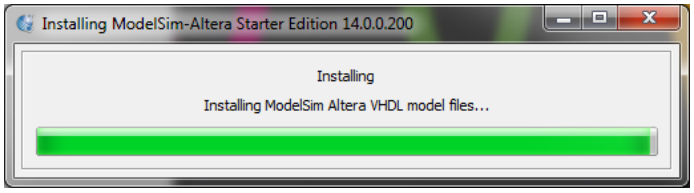


- **Th**e installation of QII Web Edition will begin:

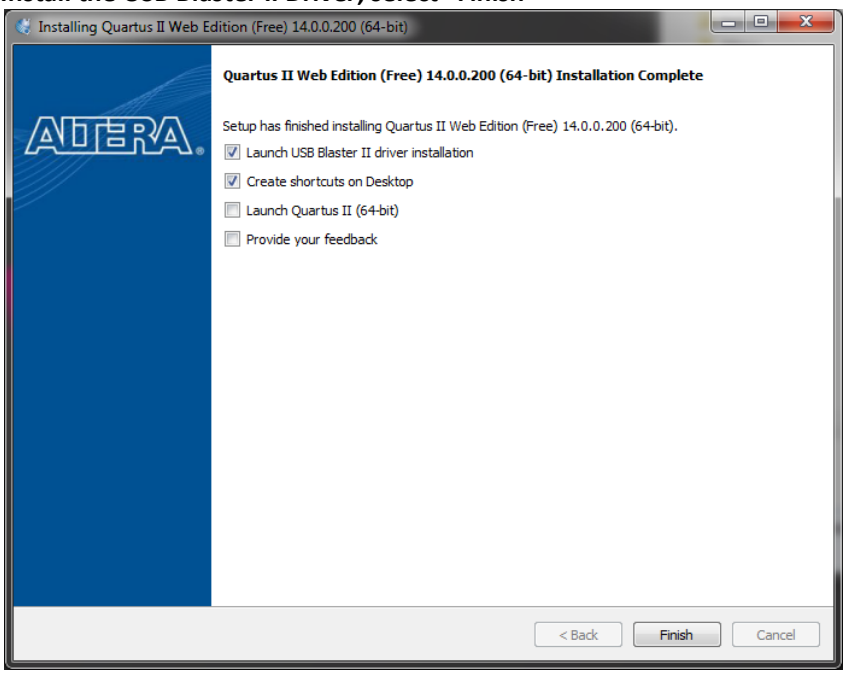


- **Th**e installation will continue with ModelSim Starter Edition:

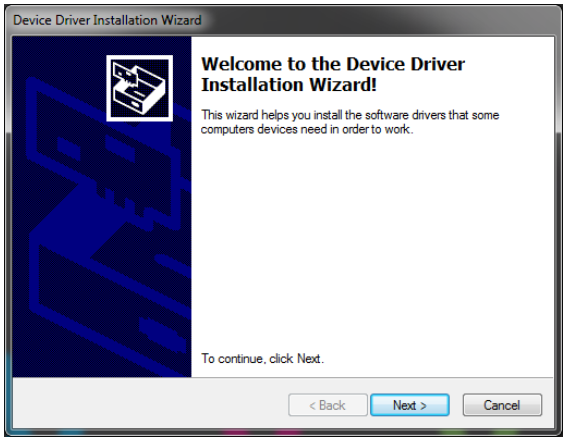


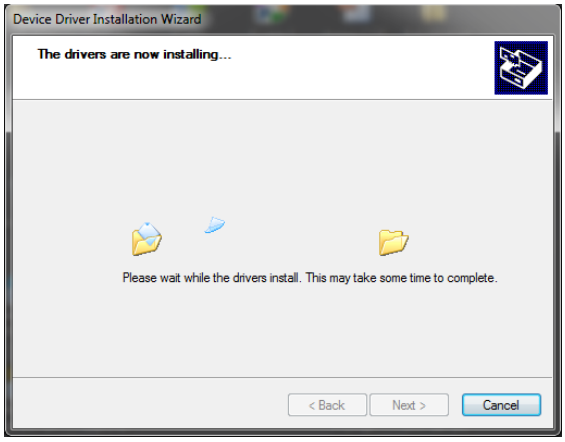


- **Install the USB Blaster II Driver, select "Finish"**

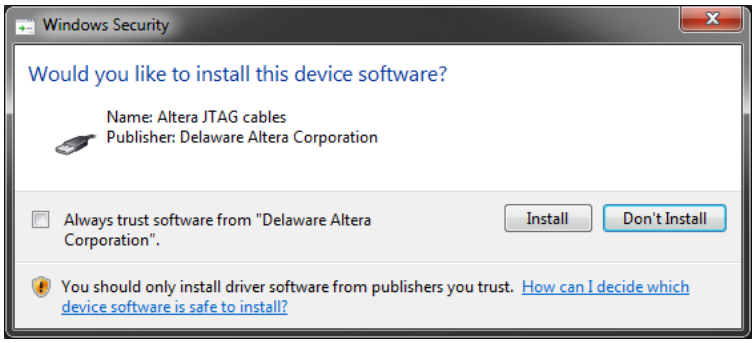


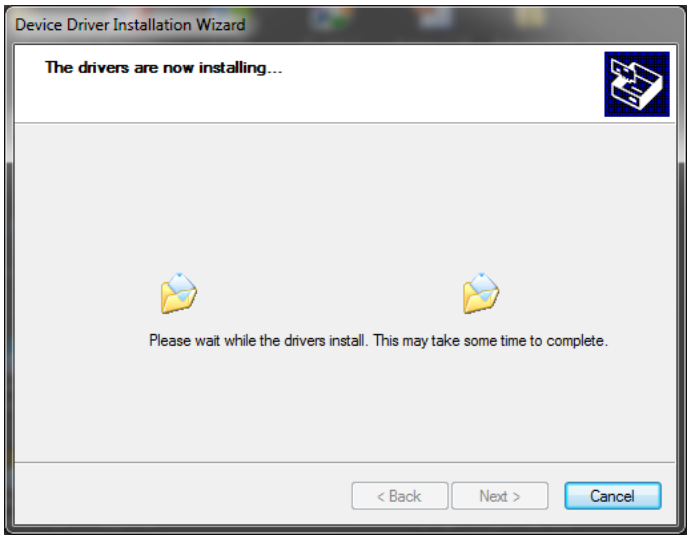
- **Select** "Next >"



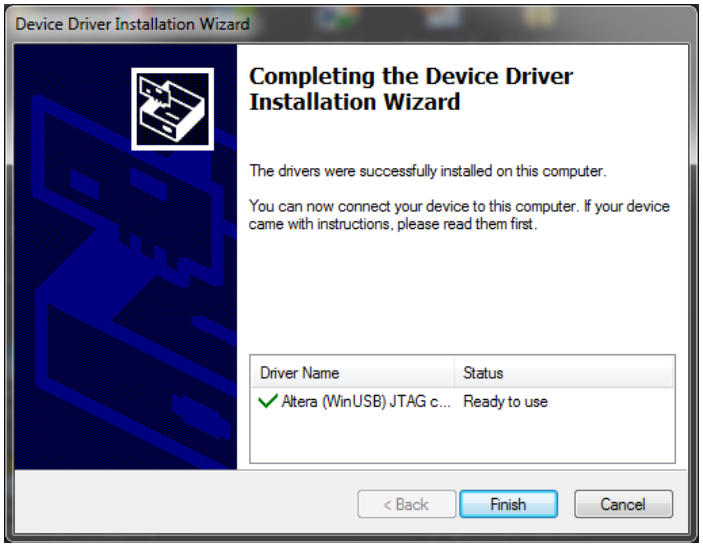


- **Select** "Install"

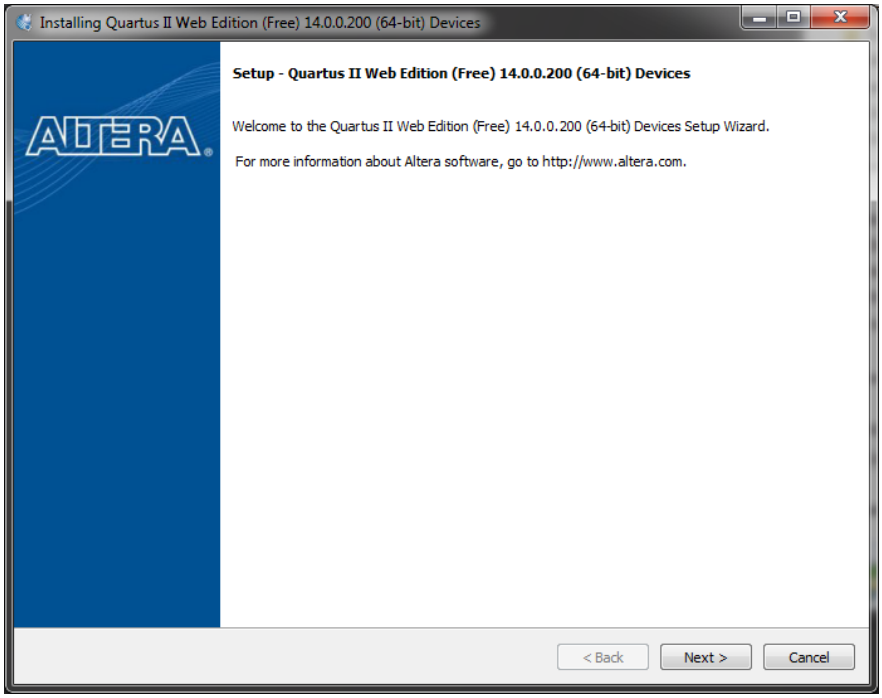




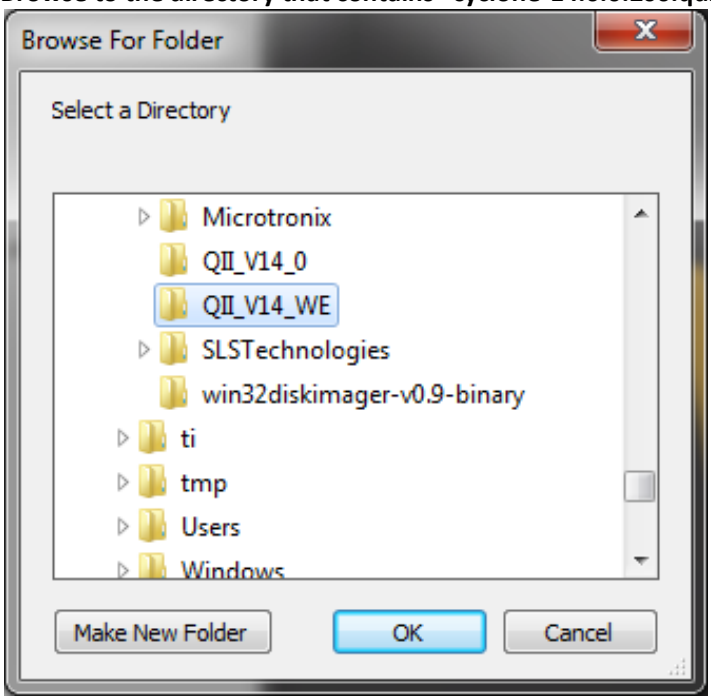
- **Select** "Finish"



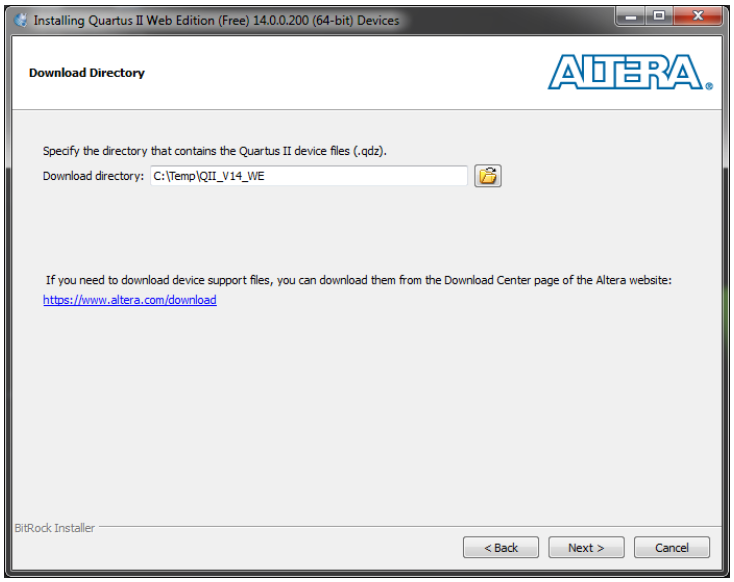
- **Next, install the Cyclone V device families**
- **Select -> All Programs -> Altera 14.0.0.200 Web Edition -> Quartus II Web Edition 14.0.0.200 (64 bit) -> Quartus II 14.0 Device Installer**
- **Select "Next >"**



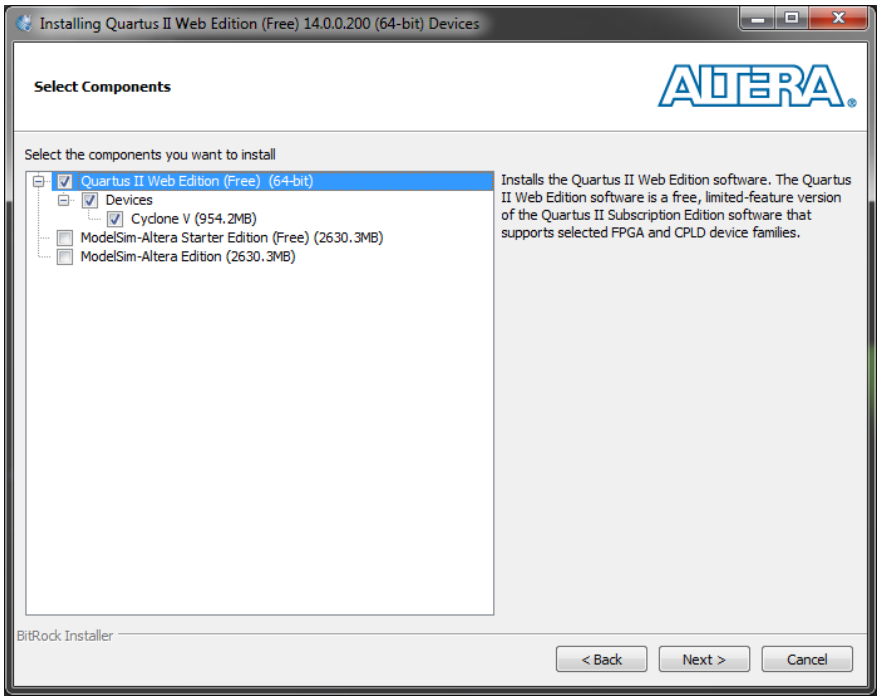
- **Browse to the directory that contains "cyclone-14.0.0.200.qdz"**



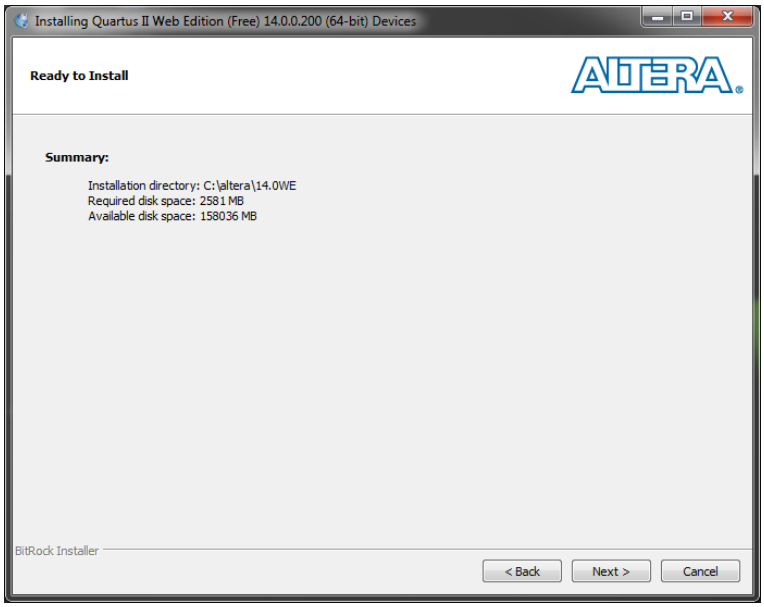
- **Select "Next >"**



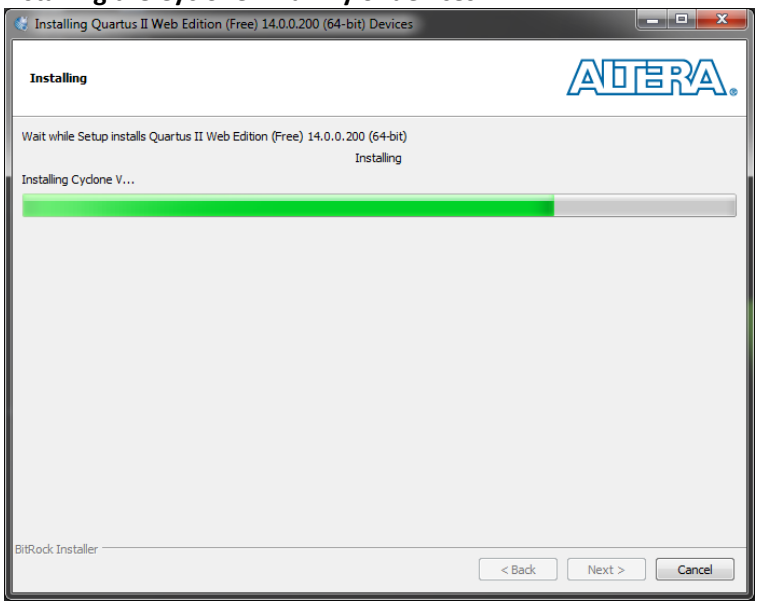
- **Select Quartus II Web Edition (Free) (64 bit) ONLY and the Cyclone V check box should then be selected. Then Select: "Next >"**



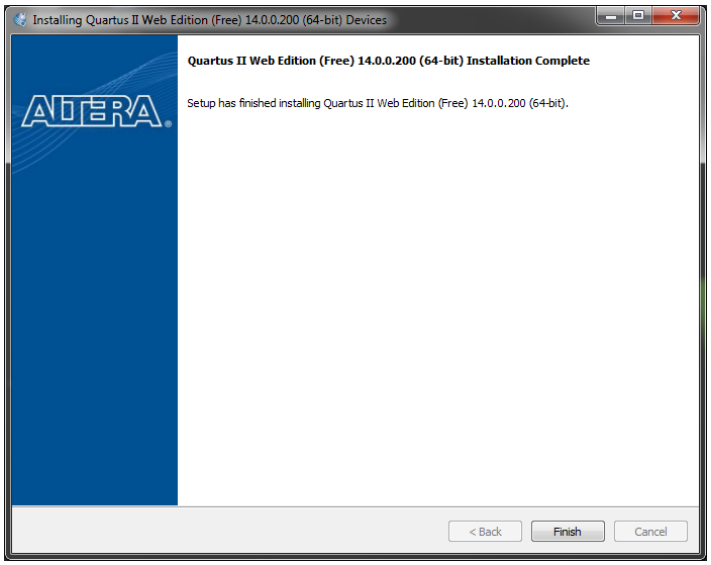
- **Select “Next >”**



- **Installing the Cyclone V Family of devices**

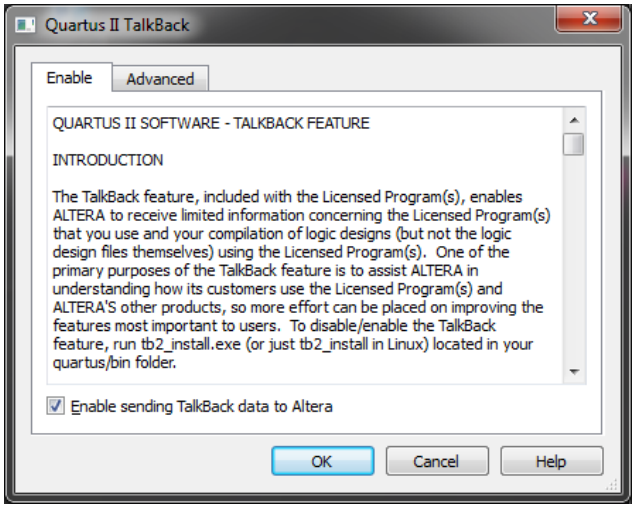


- **Select "Finish"**



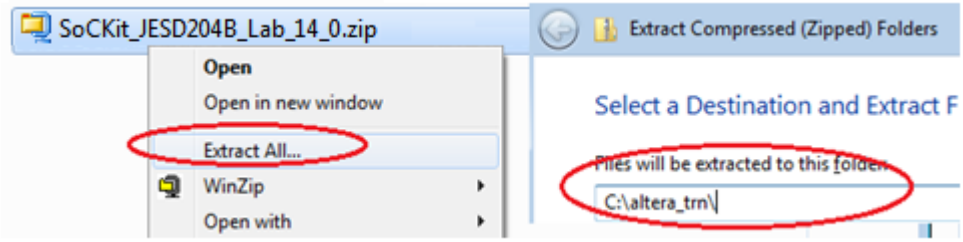
- **Select -> All Programs -> Altera 14.0.0.200 Web Edition -> Quartus II Web Edition 14.0.0.200 (64 bit) -> Quartus II 14.0 (64 bit)**

- **Enable Talkback**

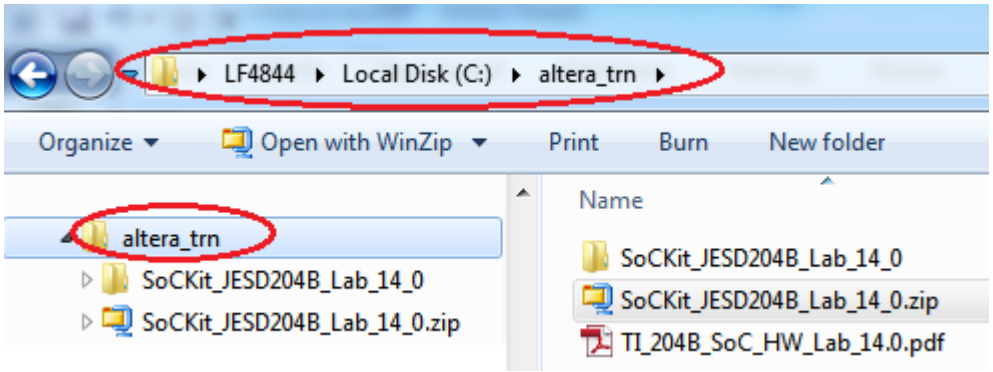


1.3 Extract the ADC34J22 JESD204B for SoCKit Lab Files.

- Create a folder **c:\altera_trn** on your PC.
- Click on the following link to download **SoCKit_JESD204B_Lab_14_0.zip**
- Save it to **c:\altera_trn** on your PC
- Extract the **SoCKit_JESD204B_Lab_14_0.zip** file to this folder



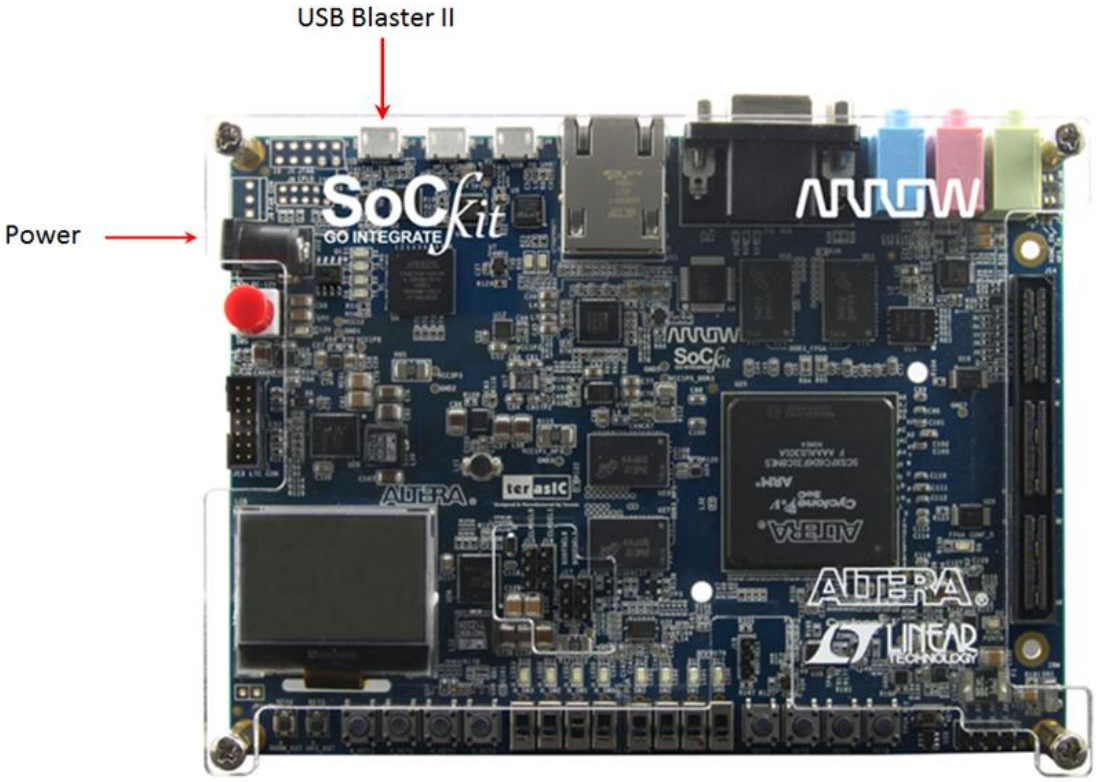
- The **c:\altera_trn** directory should look like this



1.4 Get the Cyclone V SoCKit ready for the Labs (Complete this at the Workshop)

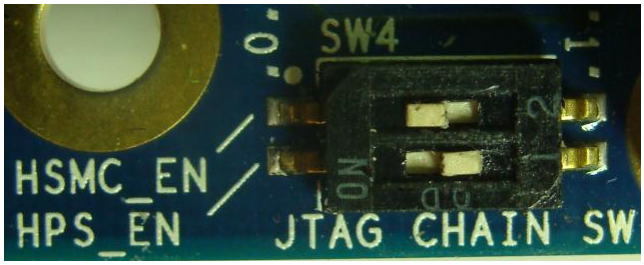
Please connect cables to the connectors shown in the diagram below. All cables are provided in your SoCKit.

- Connect the micro USB cable to the USB host connector on your laptop and to the USB Blaster II connector on the SoCKit.
- Connect the Power Supply to the Power connector on the SoCKit.

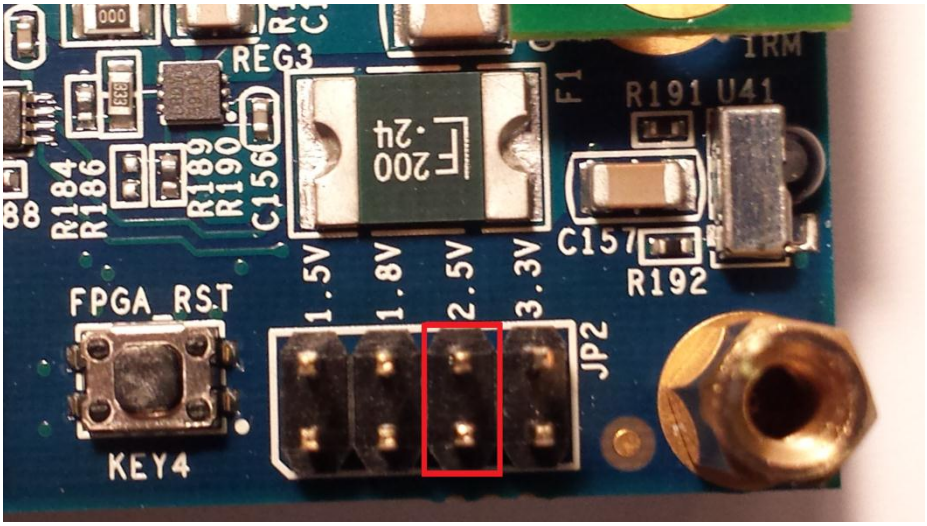


Verify that the **JTAG chain is correctly configured**. The **JTAG chain switch** is located in to the right of the **green audio** connector.

- **HSMC_EN** should be **disabled** (left position) and the **HPS_EN** should be **enabled** (right position).



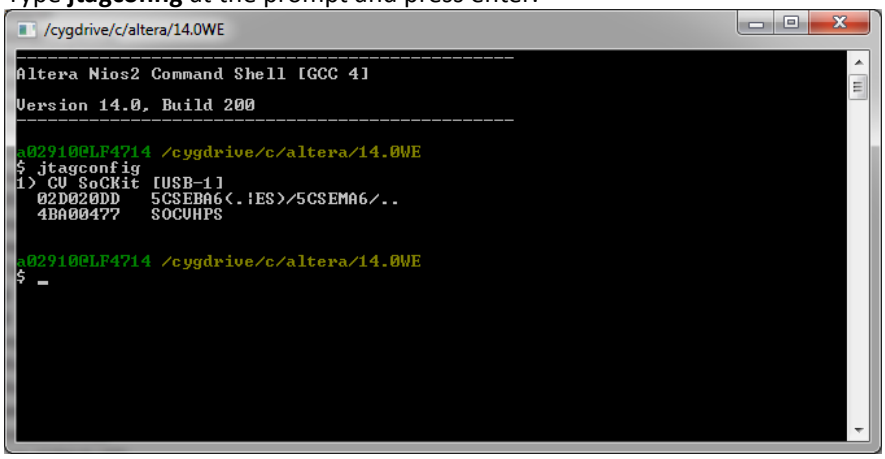
- **The Voltage for the HSMC interface/connector should be set to 2.5V**
  It is located in Lower right on front of SoCKit



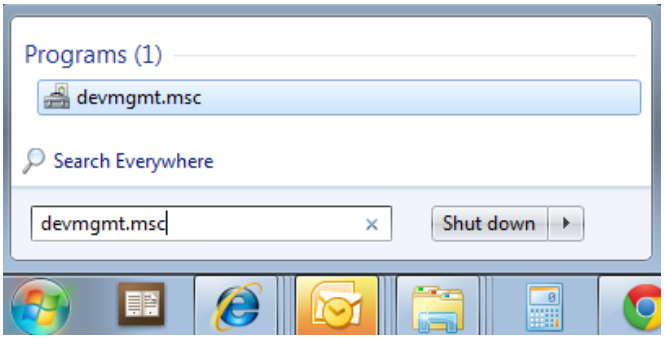
1.5 Install the USB Blaster II Device Driver (Complete if you didn't install with Quartus II in section 1.2)

- **Turn your SoCKit on.**
- Open a **NIOS II 14.0 Command** Shell**, select** **-> All Programs -> Altera 14.0.0.200 Web Edition -> NIOS II EDS 14.0.0.200 -> NIOS II 14.0 Command Shell**

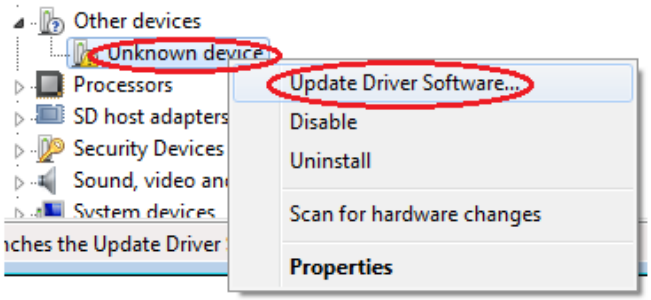
- Type **jtagconfig** at the prompt and press enter.



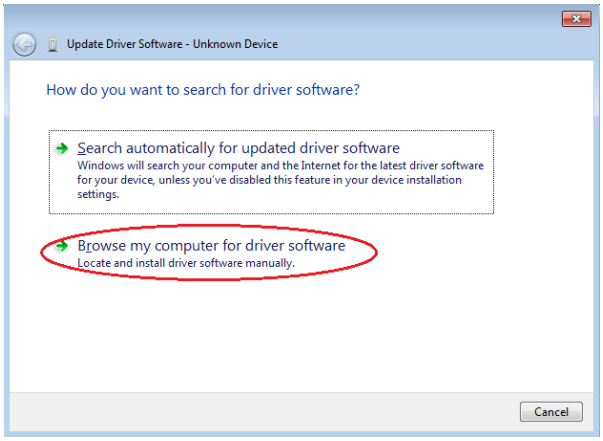
- If the jtagconfig command fails, then complete the following steps
- Press the Windows **Start** button. Enter **devmgmt.msc**. Press enter to open the Device Manager.



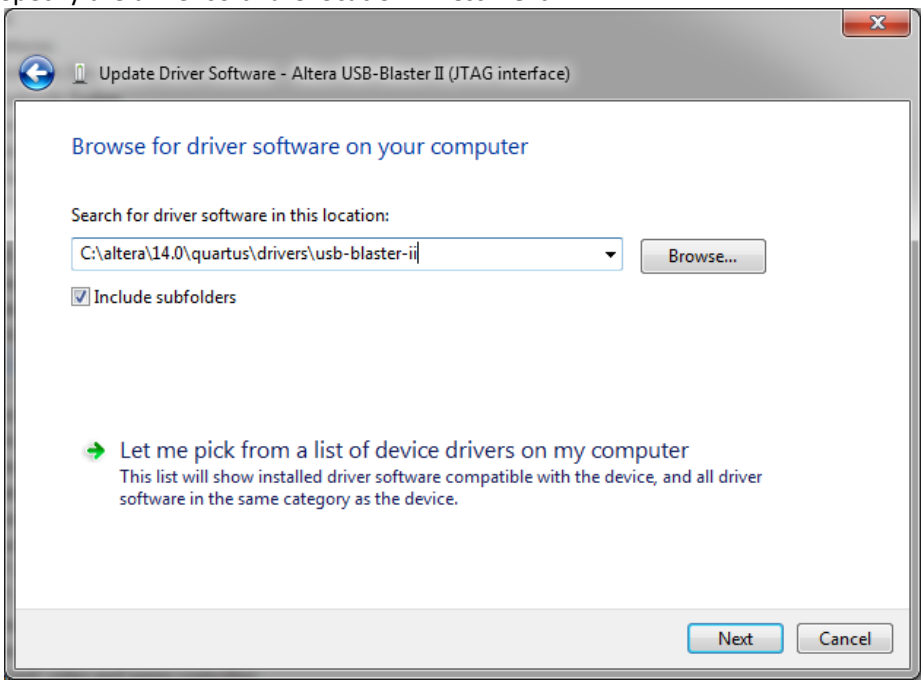
- Navigate to **Other Devices** in the Device Manager. Expand it to see **Unknown Device**
- Right click on **Unknown Device**. Select **Update Driver Software**.



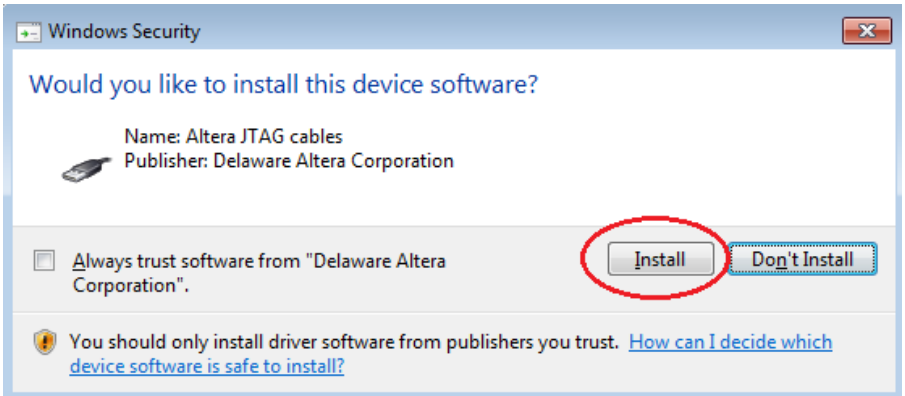
- Select **Browse my computer for driver software**.



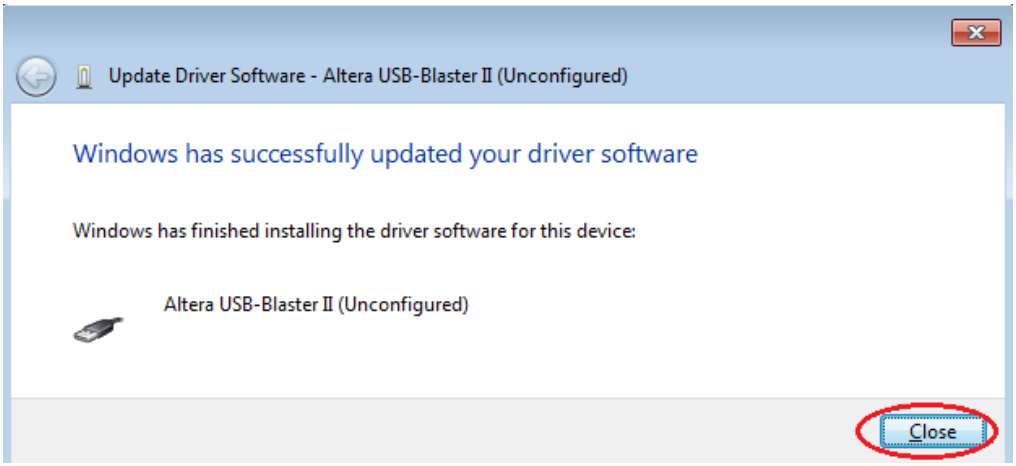
- Specify the driver software **location**. Press **Next**.



- Click Install on the next Screen

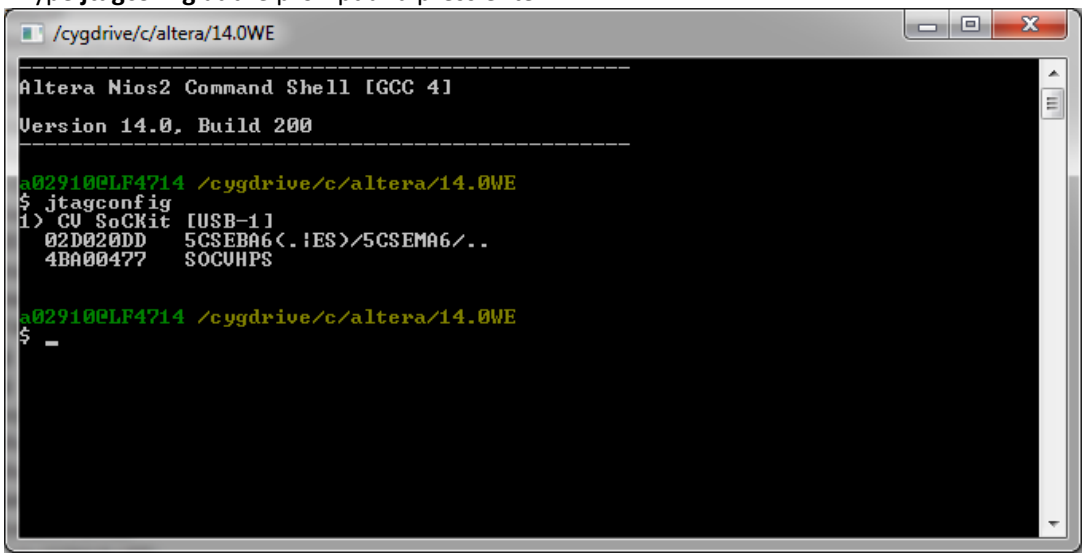


- **Wait** for the driver to **complete** its **installation**. Press Close. **Notice** that **device** is considered to be **Unconfigured**.



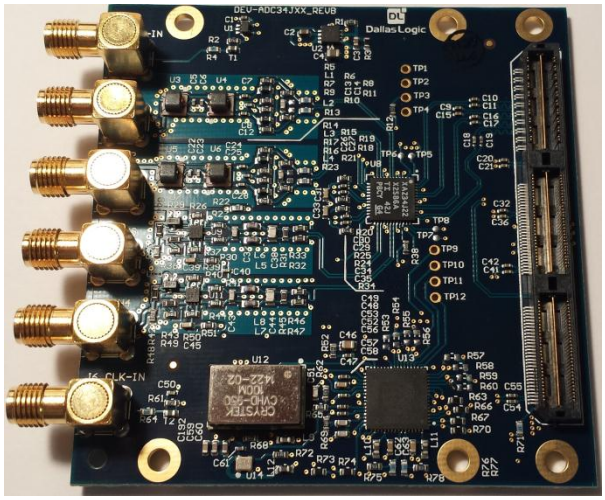
- Open a **NIOS II 14.0 Command** Shell**, select** **-> All Programs -> Altera 14.0.0.200 Web Edition -> NIOS II EDS 14.0.0.200 -> NIOS II 14.0 Command Shell**

- Type **jtagconfig** at the prompt and press enter.

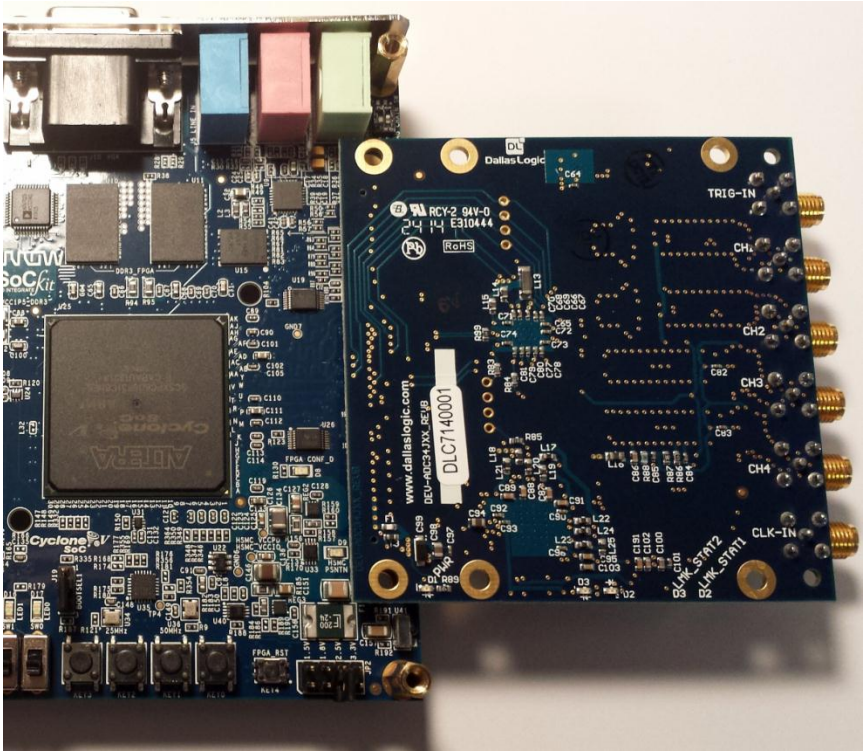


1.7 Acquire the Texas Instruments DEV-ADC34J22 JESD204B Evaluation Module

Order DEV-ADC34J22 from Arrow Electronics



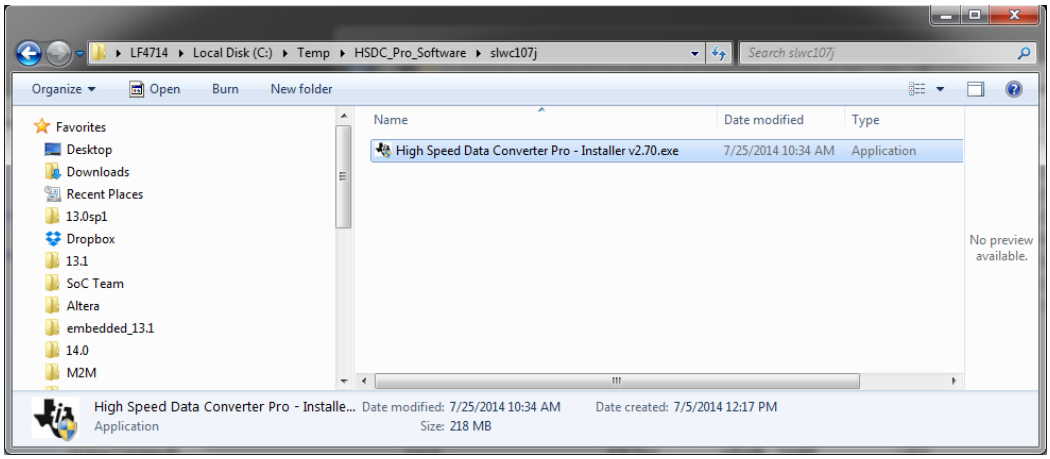
1.8 Connect the DEV-ADC34J22 JESD204B Evaluation Module to the SoCKit



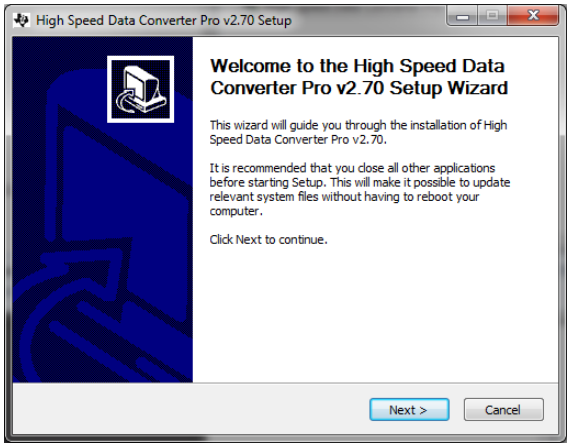
1.9 Install Texas Instrument's High Speed Data Converter Pro

- Download High Speed Data Converter Pro Software for Windows XP/7
  [High-Speed Data Converter Pro Software]
  [High-Speed Data Converter Pro GUI User Guide]

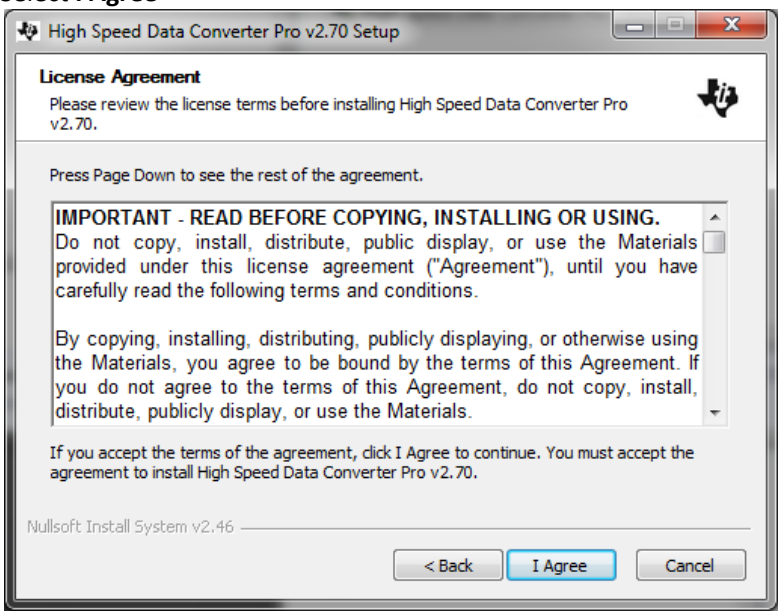
- Save to a temporary directory on your workstation
- Install High Speed Data Converter Pro Software by double clicking on the installer



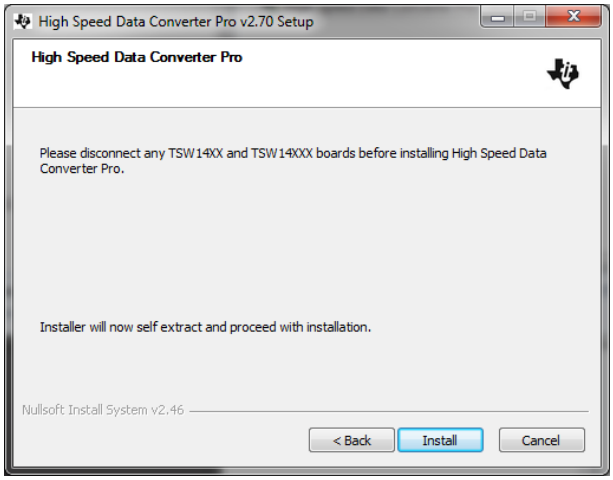
- Select **Next**

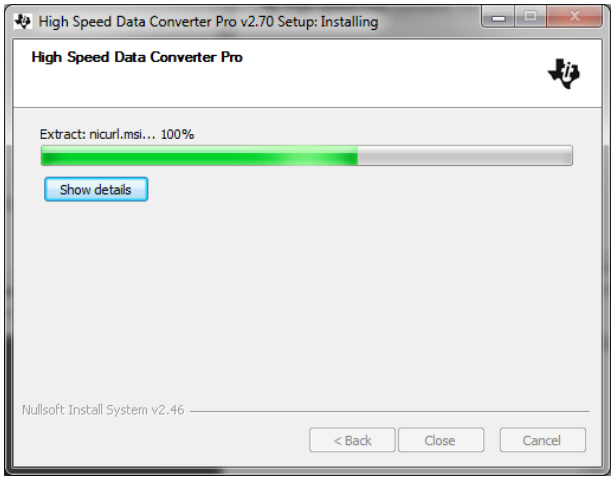


- Select **I Agree**

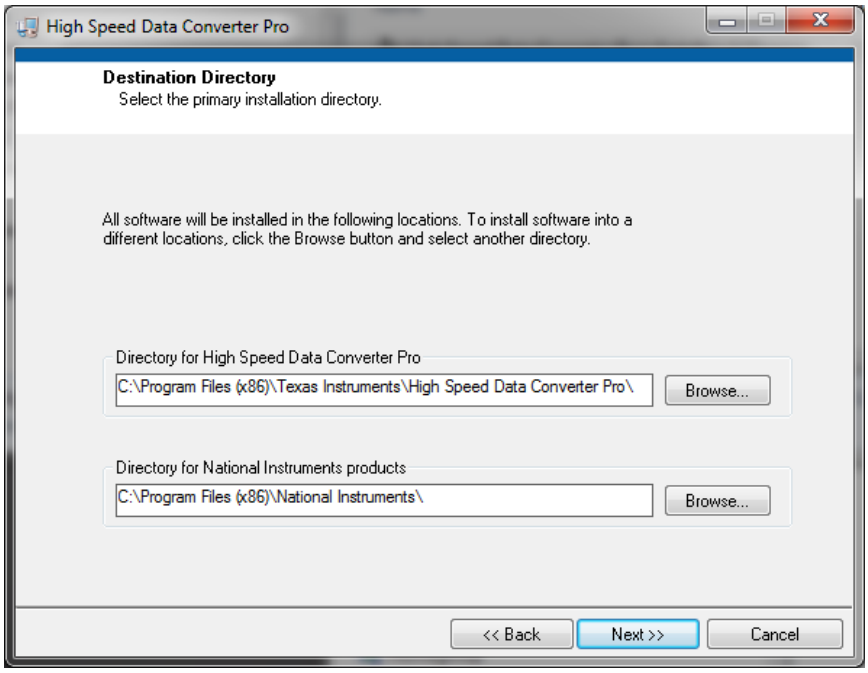


- Select **Install**

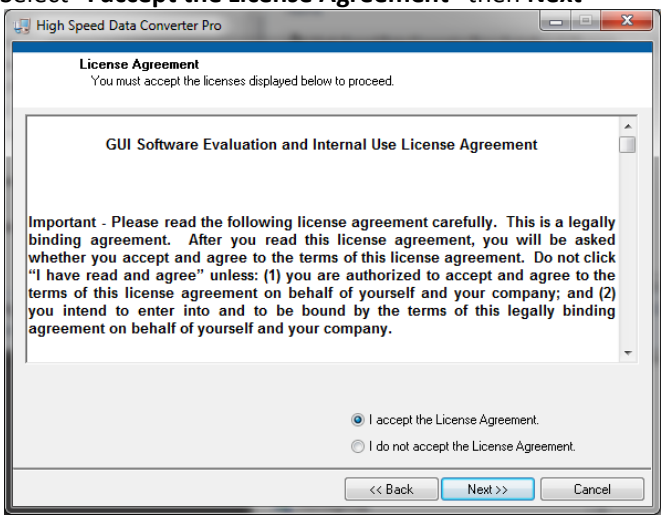




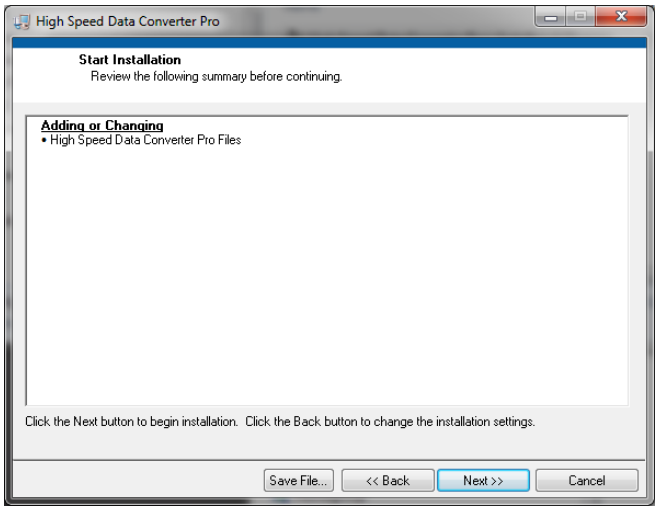
- Select **Next**



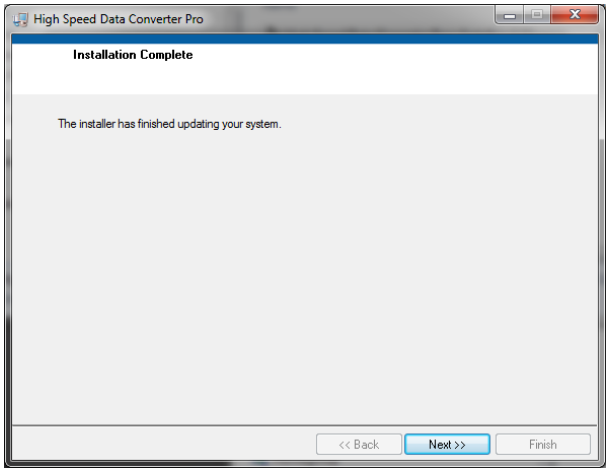
- Select "**I accept the License Agreement**" then **Next**

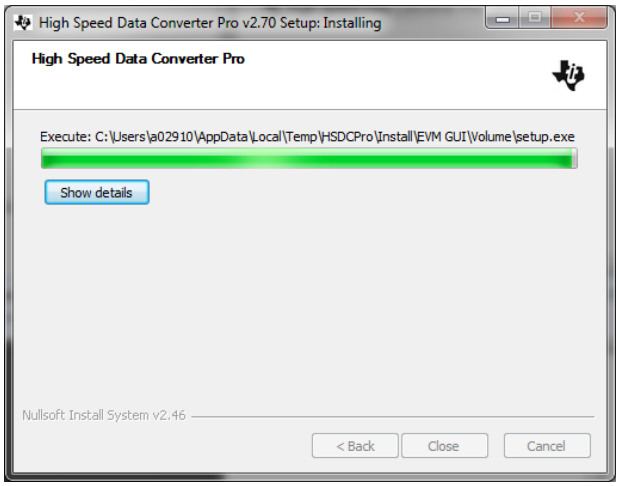


- Select **Next**

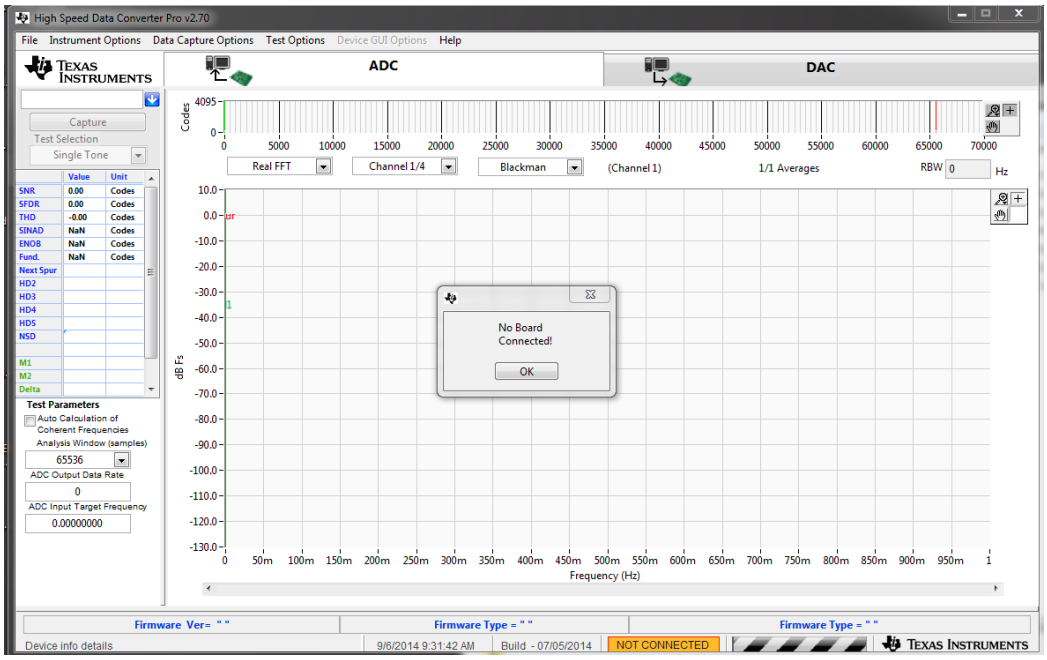


- Select **Next**





- Open High Speed Data Converter Pro, **select** **-> All Programs -> Texas Instruments ->** High Speed Data Converter Pro



- Select “OK”
- Close High Speed Data Converter Pro

CONGRATULATIONS!!

You have just completed all the setup and installation requirements and are now ready to examine the system-level design.

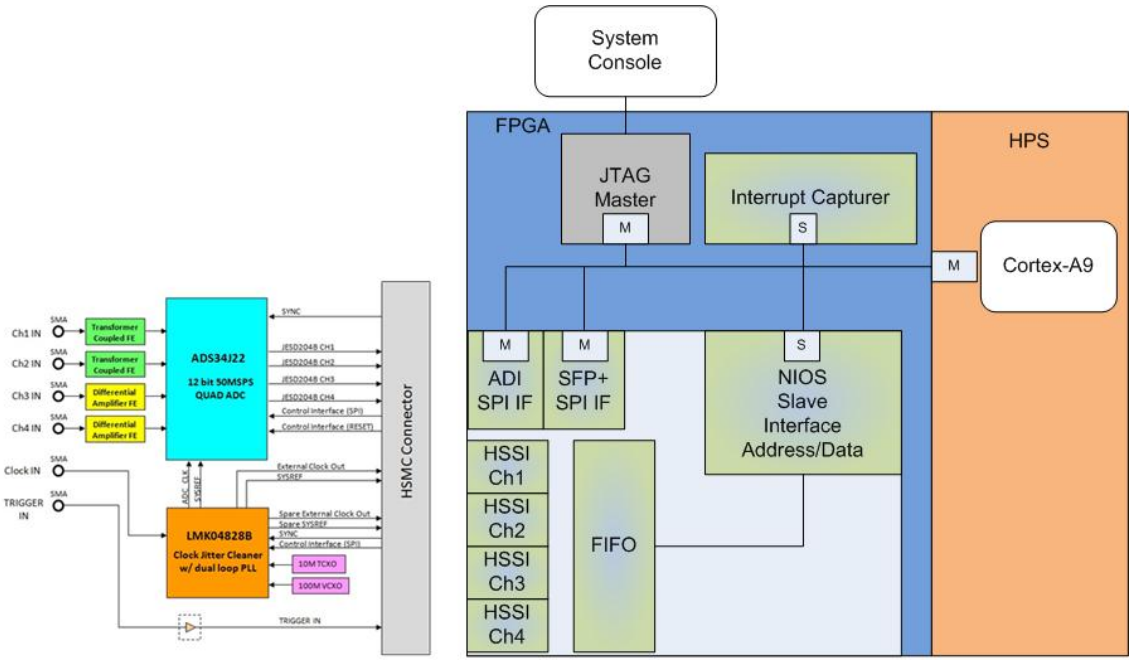
MODULE 2. Examine the System Design

Module Objective

In this module you will review the architecture of the design that was created in Qsys. You will also examine the layout of the SoCKit and a block diagram of the HSMC ADS34J22 Module. Developing software for an Altera SoC requires an understanding of the design flow of the Qsys system integration tool. Typically, a design starts with system requirements. These system requirements become inputs to the system definition. System definition is the first step for implementation in the design flow process.

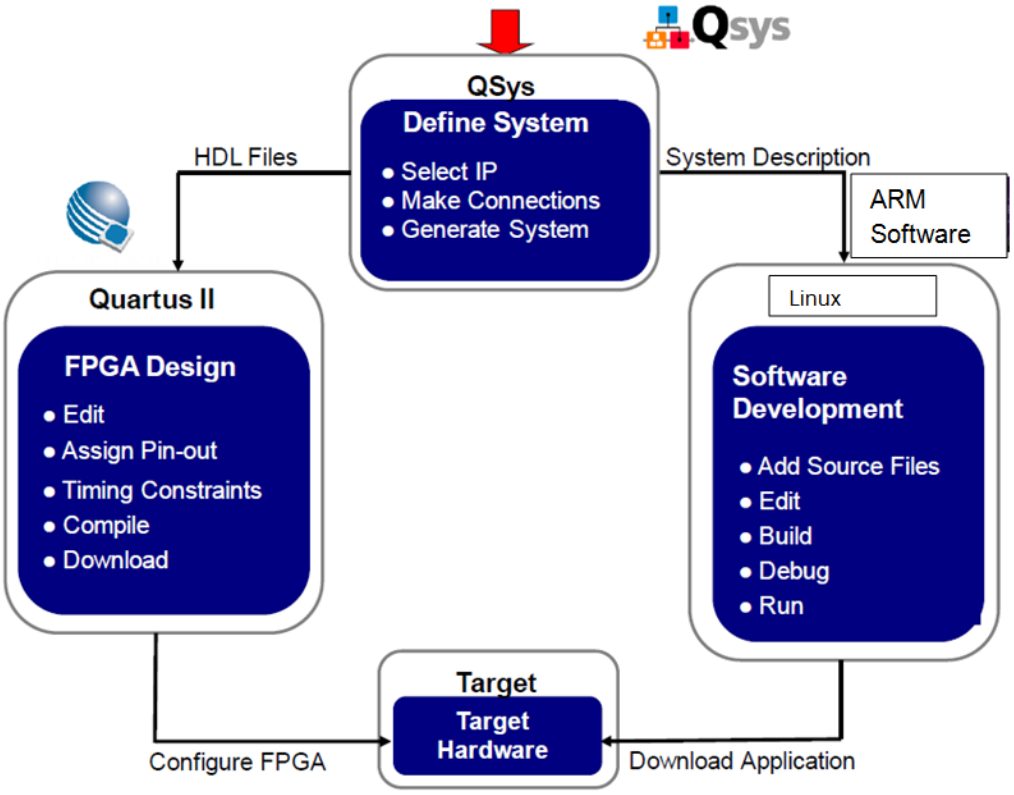
2.1 System Architecture

There are many components on the SoCKit that can be used in a system design, including the LCD, flash, Audio DACs, and IR. The system that has been completed in Qsys is built by using a standard library of re-useable IP blocks plus the JESD204B IP core from MTI. The orange section of this diagram is the HPS section, while the blue section is the FPGA section. The HPS section can be configured in the HPS component in Qsys; and is utilized in the interface to the HSMC ADC34J22 Module.



Please note for this lab the HPS will not be utilized to evaluate the data from the ADC34J22; but the JTAG master will be utilized to display the data in SignalTap (Embedded Logic Analyzer) using System Console (a Tcl based tool).

2.2 Examine the System Tool Flow

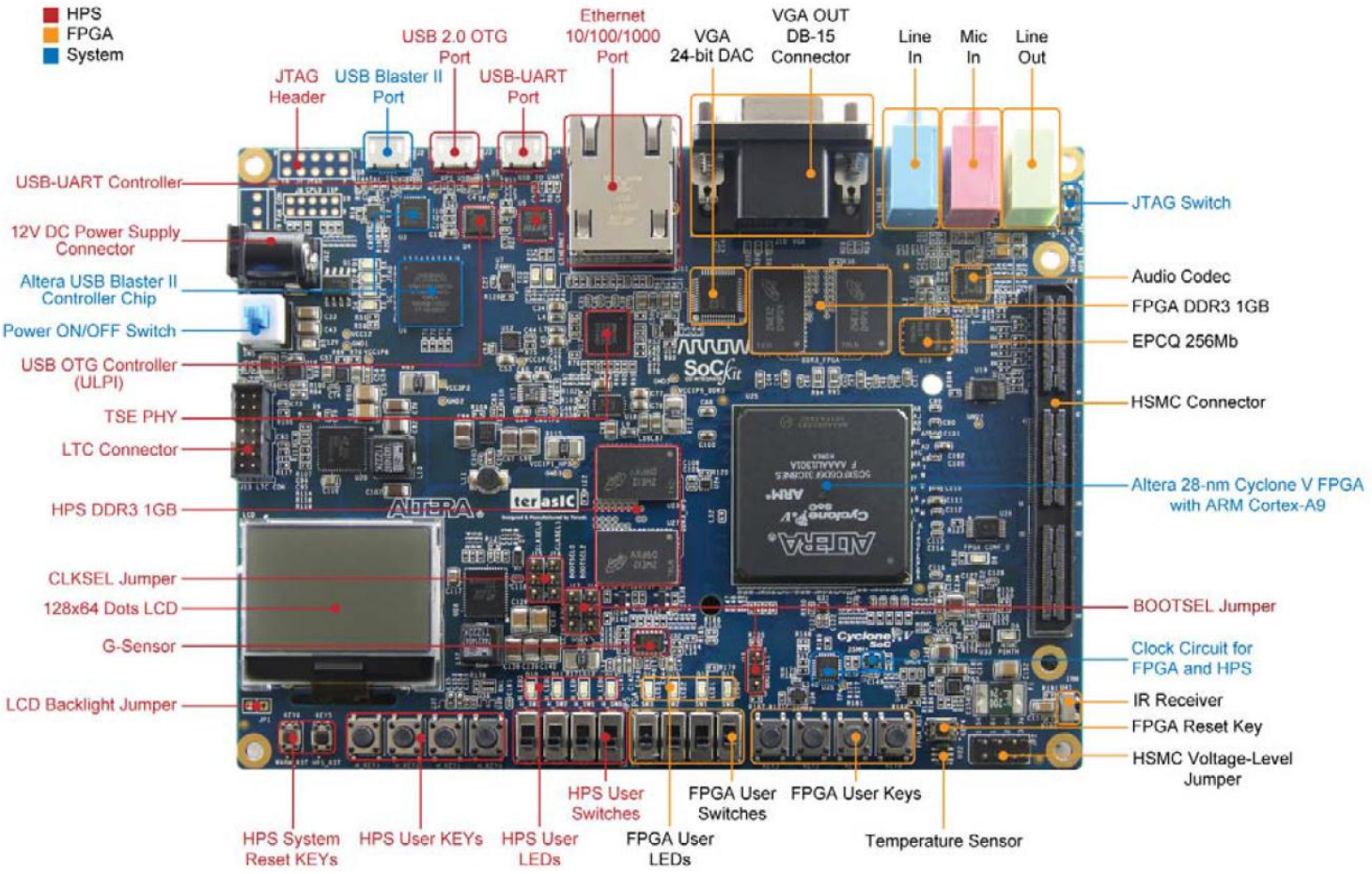


- Qsys also generates the HDL files (Verilog or VHDL) for the defined system. These HDL files are then used by Quartus II to compile and generate a set of files that defines the hardware system. Along with the HDL files; this set of files includes the Tcl (Tool Command Language) files that define dedicated pin locations for selected HPS peripherals, the Tcl files that define the Multiport Memory Controller in the HPS & FPGA, and the QIP files that include: selected IP and SDC (Synopsis Design Constraint files) utilized by TimeQuest to constrain the complete system design.

- Quartus II will then generate a simple SOF (SRAM Object File) image that is used to configure the FPGA.

2.3 Examine Arrow's Cyclone V SoCKit

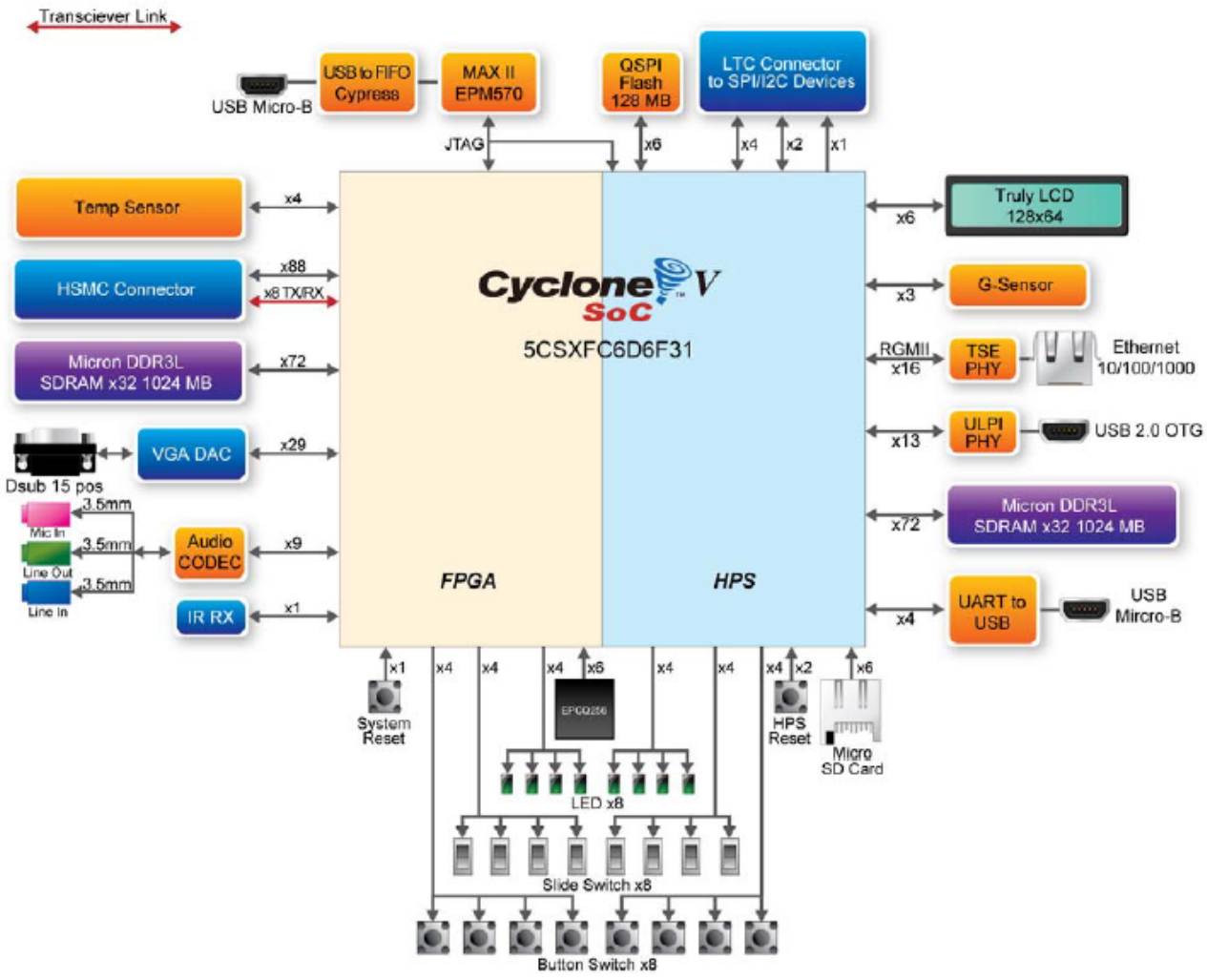
Examine the components on the Cyclone V SoC board hardware:



2.4 Block Diagram of the SoCKit

There are many components included on the SoCKit, including the LCD, flash, Audio DACs, and IR.

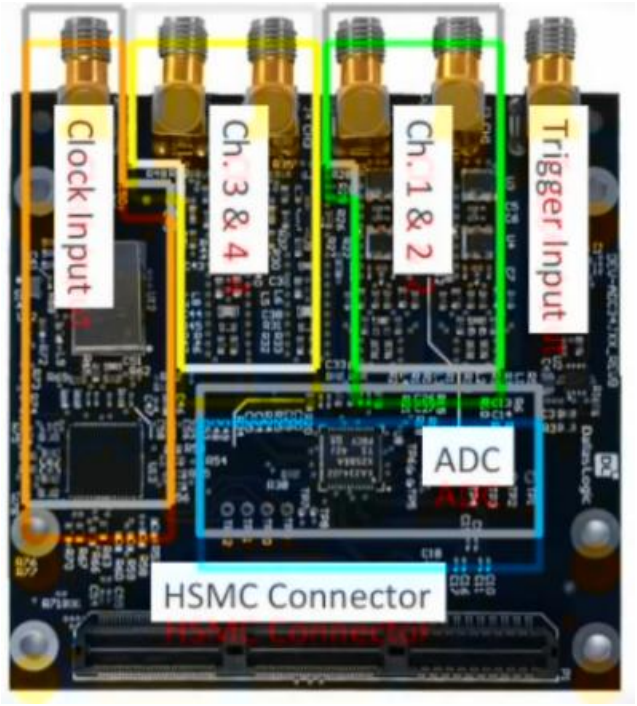
A block diagram of the board:



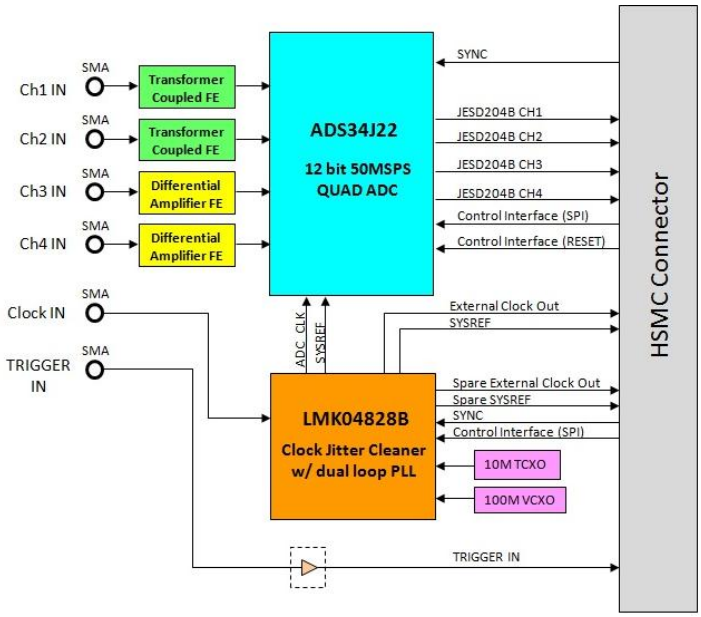
2.5 Examine the DEV-ADC34J22 Development Kit from Dallas Logic

The DEV-ADC34J22 is a four-channel, 50MSPS ADC Module designed to interface with Altera's HSMC standard interface. The DEV-ADC34J22 features TI's new JESD204B compliant ADC34J22 Analog Digital Converter (ADC), with clock conditioning using TI's LMK04828B jitter cleaner. It provides single-ended DC coupled inputs on two of the four channels through TI's THS4541 850MHz BW fully differential amplifier and the other two input channels are AC coupled.

The module offers six front panel SMA connectors: 1 EXT trigger, 1 EXT clock and 4 Analog Input Channels, and an on board 10MHz TCXO for stand-alone clock generation, with a 100MHz VCXO used in conjunction with the LMK04828B for reference clock jitter cleaning. The ADC34J22 and the LMK04828B are completely configurable via Altera's Cyclone V SOC FPGA with its embedded ARM Cortex A9 processors. The DEV-ADC34J22 supports a wide range of applications and offers two RF (AC coupled) channels and two Analog (DC coupled) channels.



2.6 Block Diagram of the Texas Instruments DEV-ADC34J22 JESD204B Evaluation Module



CONGRATULATIONS!!

You have just completed the examination of the system-level design

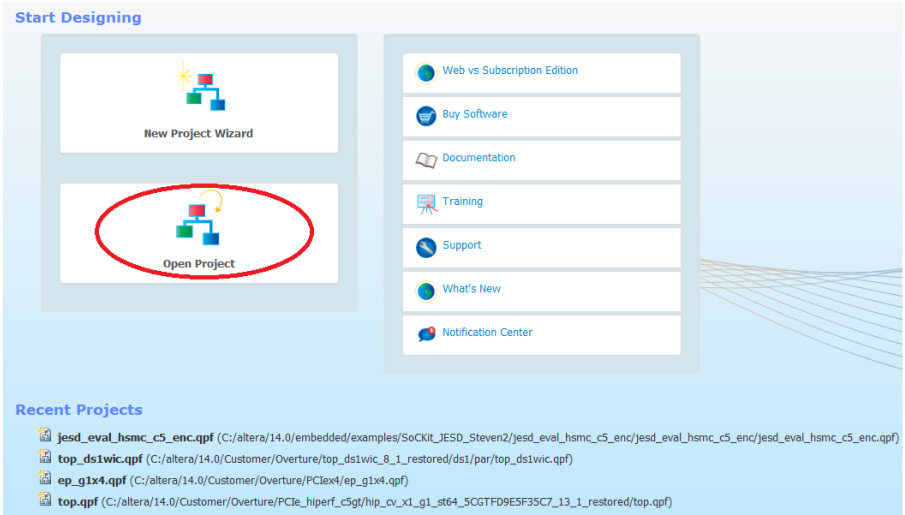
MODULE 3. Data acquisition flow using SoCKit, DEV-ADC34J22 and System Console

In this section, you will examine the example design in Quartus and Qsys.

3.1 Launch and Examine the Quartus II Project

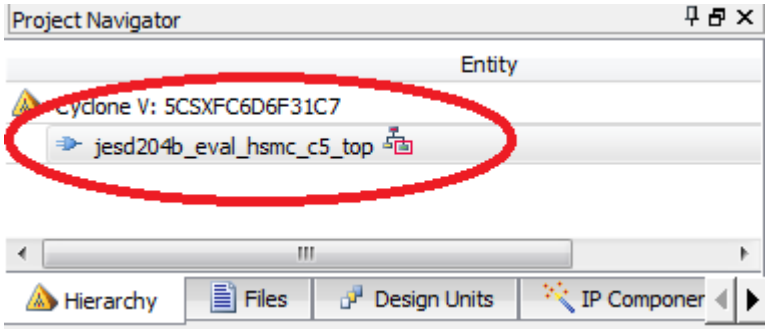
In this section, you will open a Quartus II project that contains the system that connects to the ADC34J22 converter. You will briefly examine the design in Quartus and Qsys. You will use a dashboard in System Console to program the ADC34J22 converter and SignalTap to review the received data.

- Launch the **Quartus II v14.0** software: **Select** **-> All Programs -> Altera 14.0.0.200 Web Edition -> Quartus II Web Edition 14.0.0.200 (64 bit) -> Quartus II 14.0 (64 bit)**
- A splash screen will appear. Select **Open Existing Project**:
- Browse to the directory: **C:\altera_trn\SoCKit_JESD204B_Lab_14_0**
- Select **jesd_eval_hsmc_c5_enc.qpf** and then select **Open.**



If you close the splash screen without opening the project:

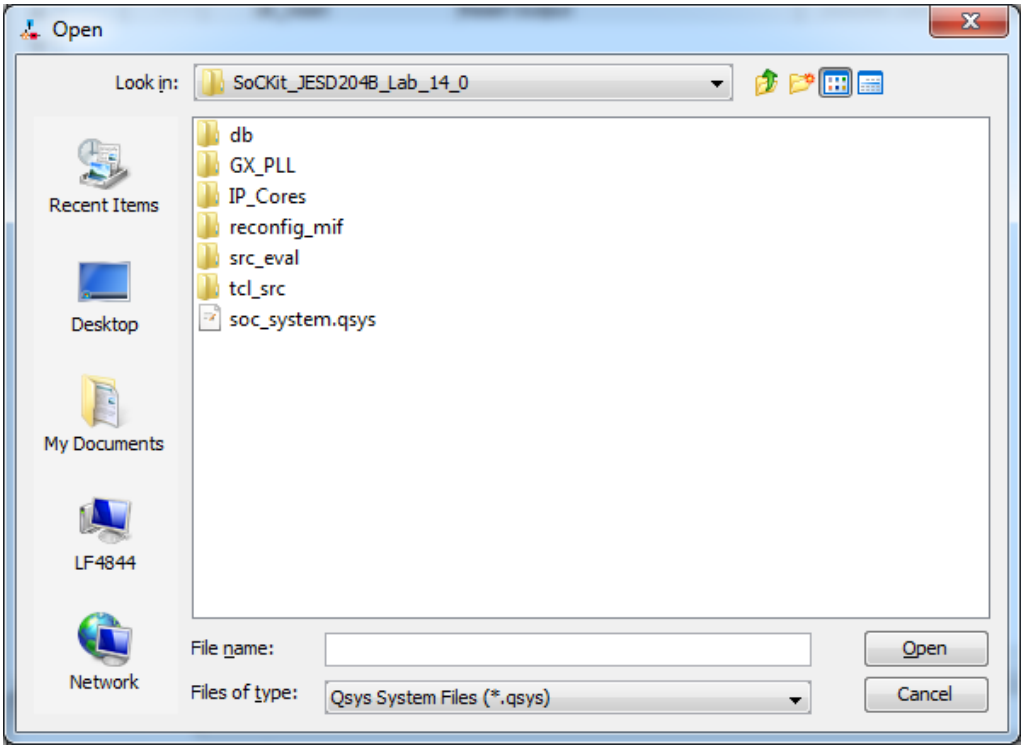
- Select **File** -> **Open Project** and browse to the directory **c:\altera_trn\SoCKit\SoCKit_HW_lab_14.0**.
- Select **soc_system.qpf**.
- The Quartus II project will open. The project already contains a top level VHDL file (jesd204b_eval_hsmc**.vhd**).
- Please take a look at the top level file. To do this, **double click** on the jesd204b_eval_hsmc icon in the Project navigator Window OR select: **File** -> **Open** and browse to the **..\top** directory and open jesd204b_eval_hsmc**.vhd**



- The jesd204b_eval_hsmc**.vhd** contains all of the I/O for the HPS instance as well as all the FPGA I/O. **In addition**, you will find the **instance** for the **Qsys component**, **soc_system** at line 515 of the file.
- The jesd204b evaluation core is instantiated at line 668 of the file.

3.2 Launch and Examine the Qsys system

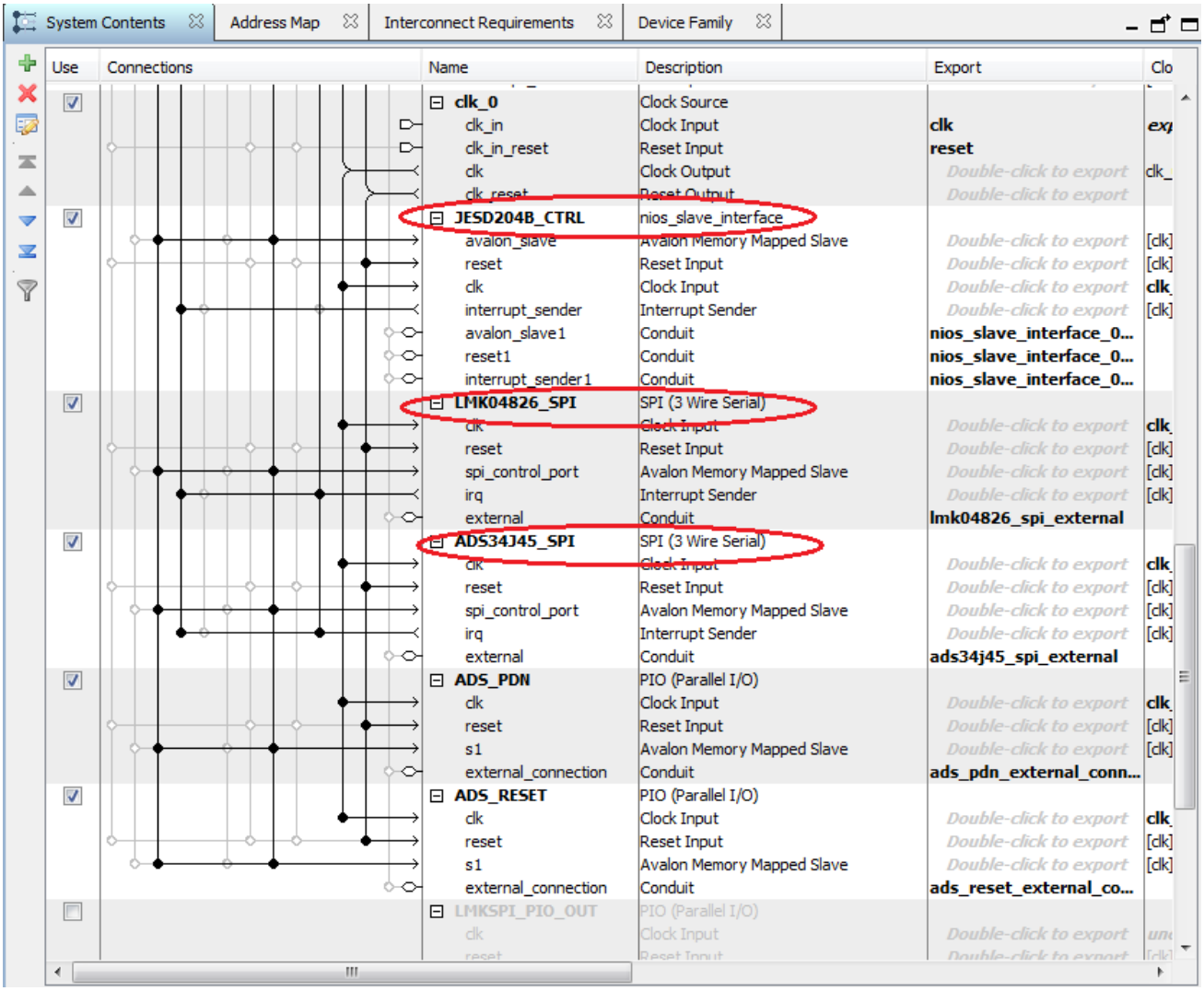
- From the **Tools** menu, select "**Qsys**". There may be a slight delay while the Qsys application launches.
- Open the File named **soc_system.qsys**



This design is based on the Golden Hardware Reference Design for the SoCKit. It has added a few peripherals that are used to provide connectivity to the JESD IP core, the ADC34J22 ADC and the LMK04826 clock jitter cleaner.

Please note the following components shown in the qsys snapshot below

- nios_slave_interface. This provides an Avalon memory mapped interface to the JESD 204B evaluation IP core.
- SPI interface. This provides an SPI control plane interface to the LMK04826 clock jitter cleaner.
- SPI interface. This provides an SPI control plane interface to the ADC34J22 ADC.

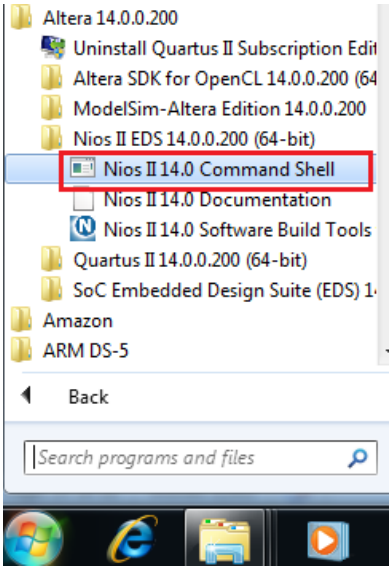


3.3 Launch SignalTap II and System Console

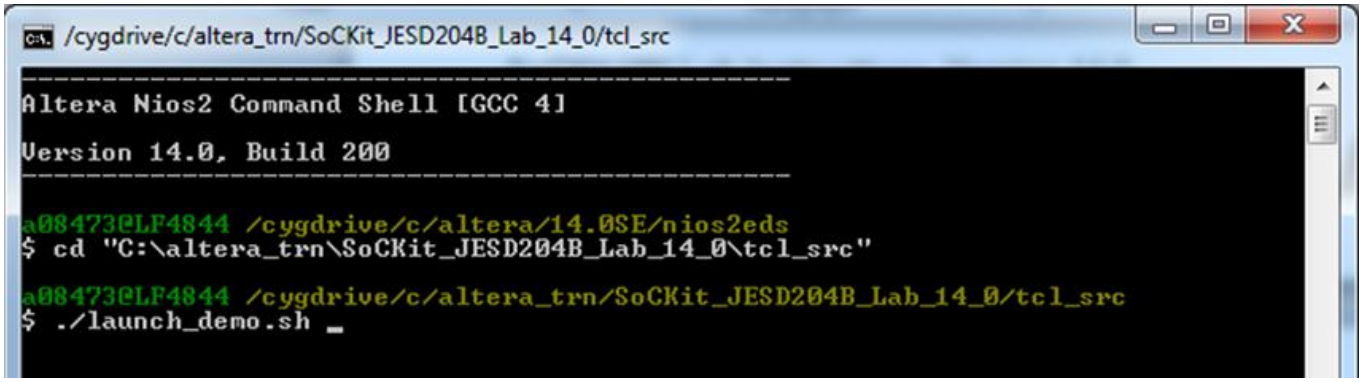
In this section you will launch Altera's SignalTap II Embedded Logic Analyzer and System Console tools. They will be used to control and monitor the ADC34J22 ADC.

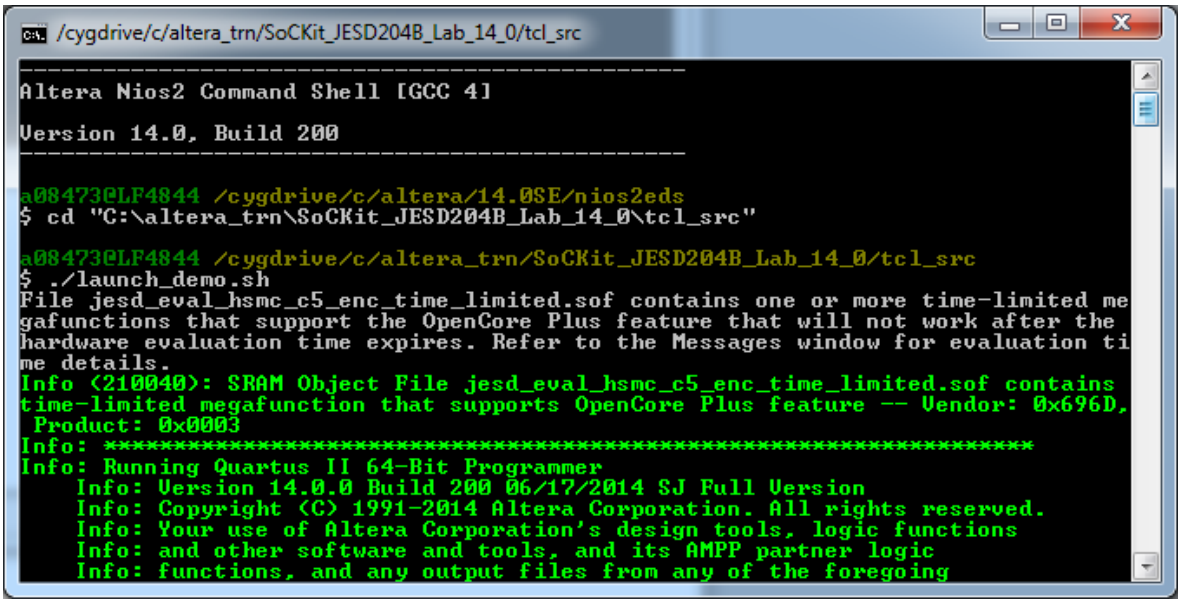
Prior to executing the next steps ensure that the SD card in the SoCKit is in the **ejected position** and that the kit has been configured as required by section **1.4**

- **Press the power button on the SoCKit.**
- Launch the **Nios II 14.0 Command Shell**: **Select** **-> All Programs -> Altera 14.0.0.200 Web Edition -> Nios II 14.0 Command Shell**

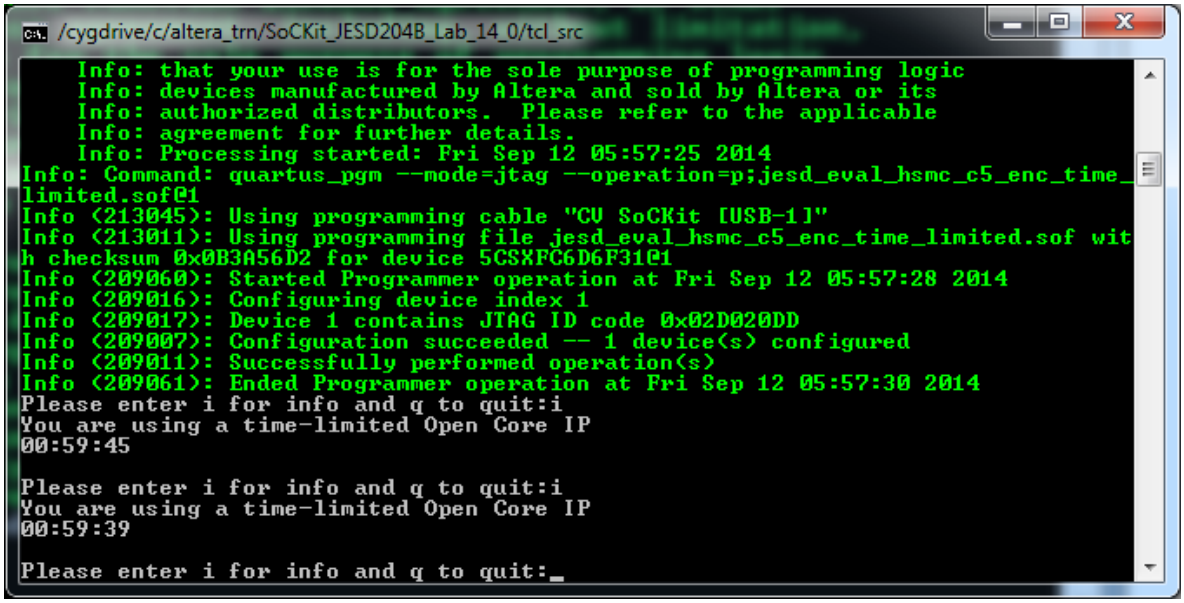


- **Change** to the current project **tcl_src** directory. Type cd **"C:\altera_trn\SoCKit_JESD204B_Lab_14_0\tcl_src"** and press **enter**.
- Use a **shell script** to launch SignalTap, System Console and program the FPGA. Type **./launch.sh** and press **enter**.





Wait at least 30 to 45 seconds for the tools to launch and the FPGA to be programmed. If you are interested you can use a text editor to examine the collection of tcl files that are used to create the JESD204B System Console Dashboard.



The sof file that was down loaded is a time limited variant. If you press "q" to quit, the core will no longer be functional and the demo will not work. The core will run for an hour if connected to this shell on the host PC. Pressing 'i' and then enter will identify how much run time is remaining (as shown above).

3.4 Capture ADC Test Pattern Data

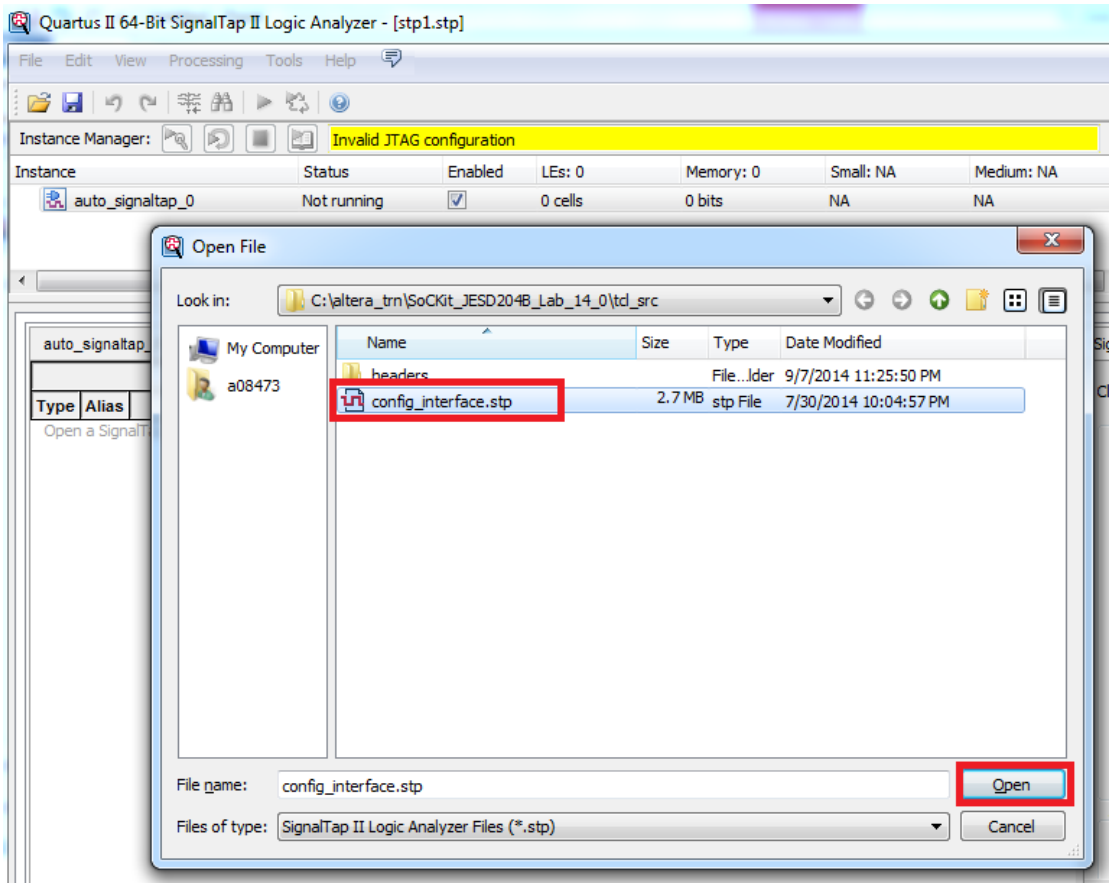
SignalTap and System Console both use the **JTAG** interface to communicate with the FPGA. **SignalTap** uses logic and memory in the FPGA to implement an embedded Logic Analyzer function. **System Console** allows the user (also via the same JTAG connection) to address the embedded memory map of peripherals designed into the FPGA target using Qsys.

The **fpga_only_master** component (which is a **JTAG to Avalon Master Bridge**) was instantiated in the Qsys design to facilitate **System Console** memory mapped **read and write accesses** to the FPGA target design.

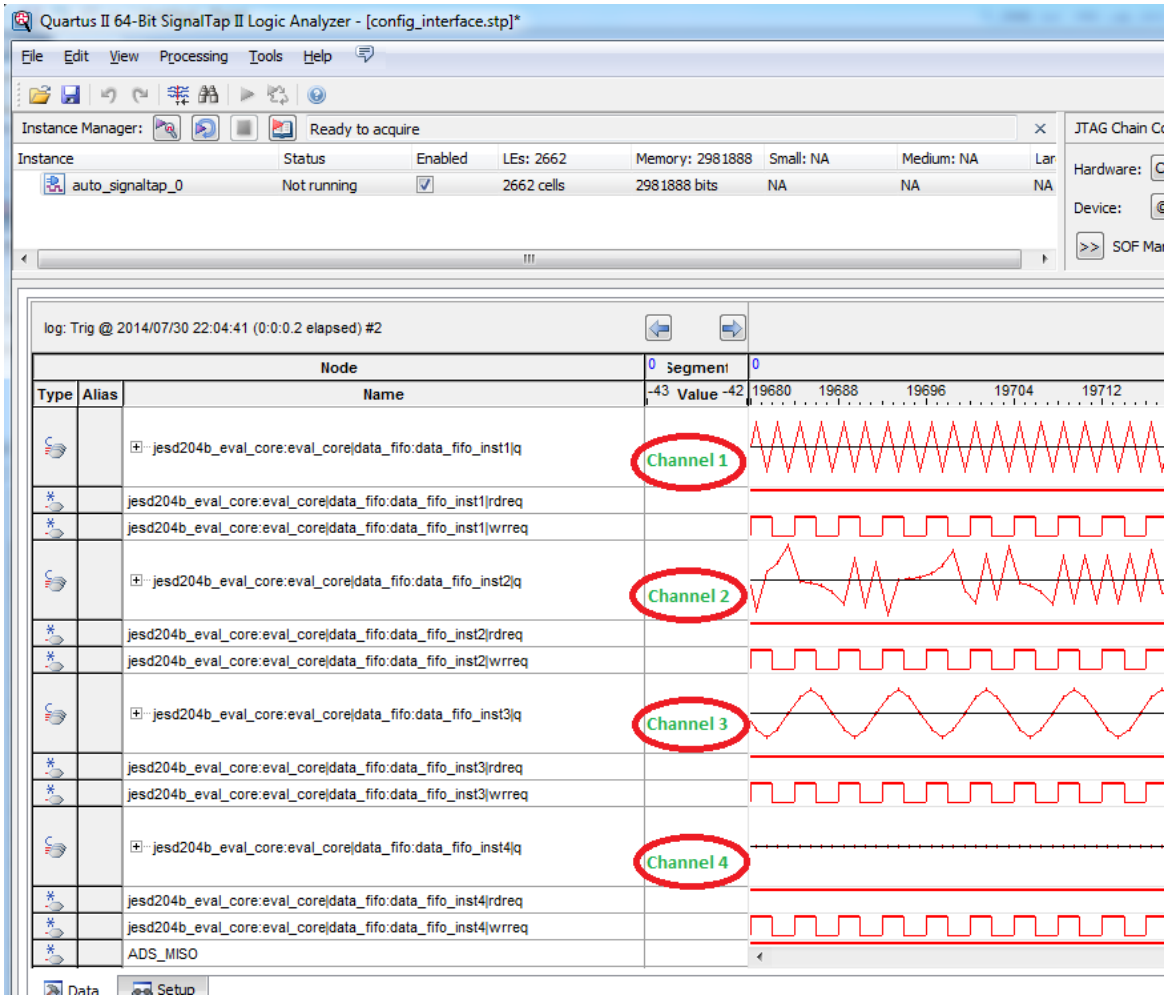
⊟ **fpga_only_master**	JTAG to Avalon Master Bridge
clk	Clock Input
clk_reset	Reset Input
master	Avalon Memory Mapped Master

Turn your attention to the **SignalTap II user interface** and open the stp setup file provided for this lab

- Open the stp file provided. File → Open File
- Select config_interface.stp



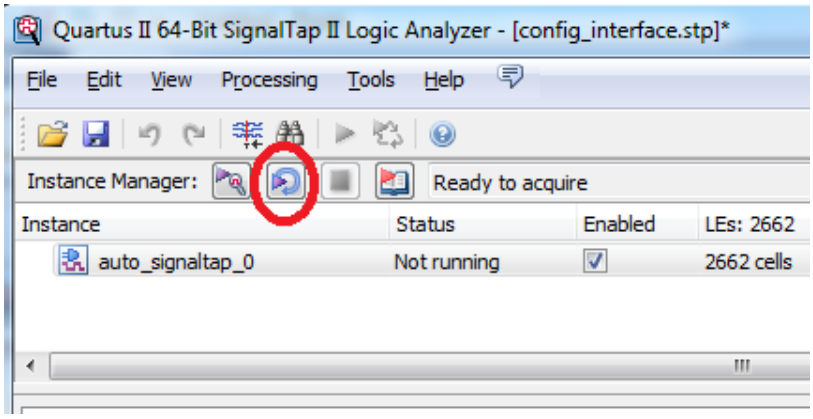
The view below is the default snapshot once the stp file has loaded. The four streaming data channels from the ADC are identified for your convenience. Streaming data from the JESD IP core is wired to individual FIFO memories for each channel. **SignalTap** will be capturing **samples** from each **FIFO and** displaying it as shown in the **snapshot below.**



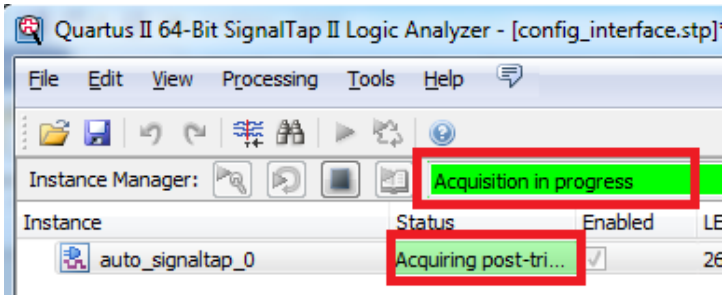
Note that the channels are also referred to as A through D in the System Console dashboard

Place SignalTap II in an active data acquisition mode.

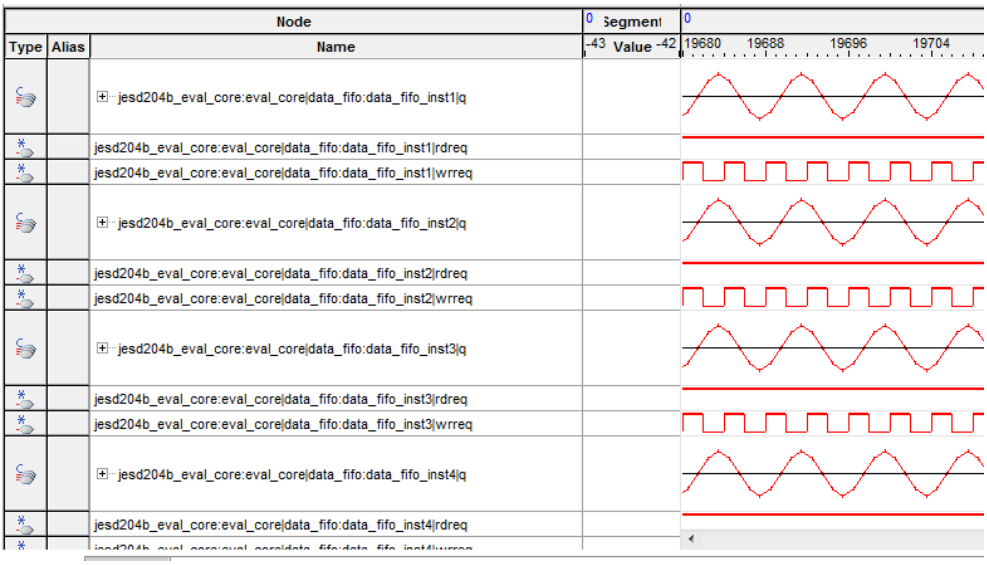
- Press the **Autorun Analysis** button to start data aquisitions



Notice that the Analyzer **status** changes to **Acquisition in progress**



The Analyzer will now continue to capture and display **ADC data** since there is no **defined trigger**. The ADC has been configured by default to send 8-point sine wave data in a Test pattern mode (as seen below)



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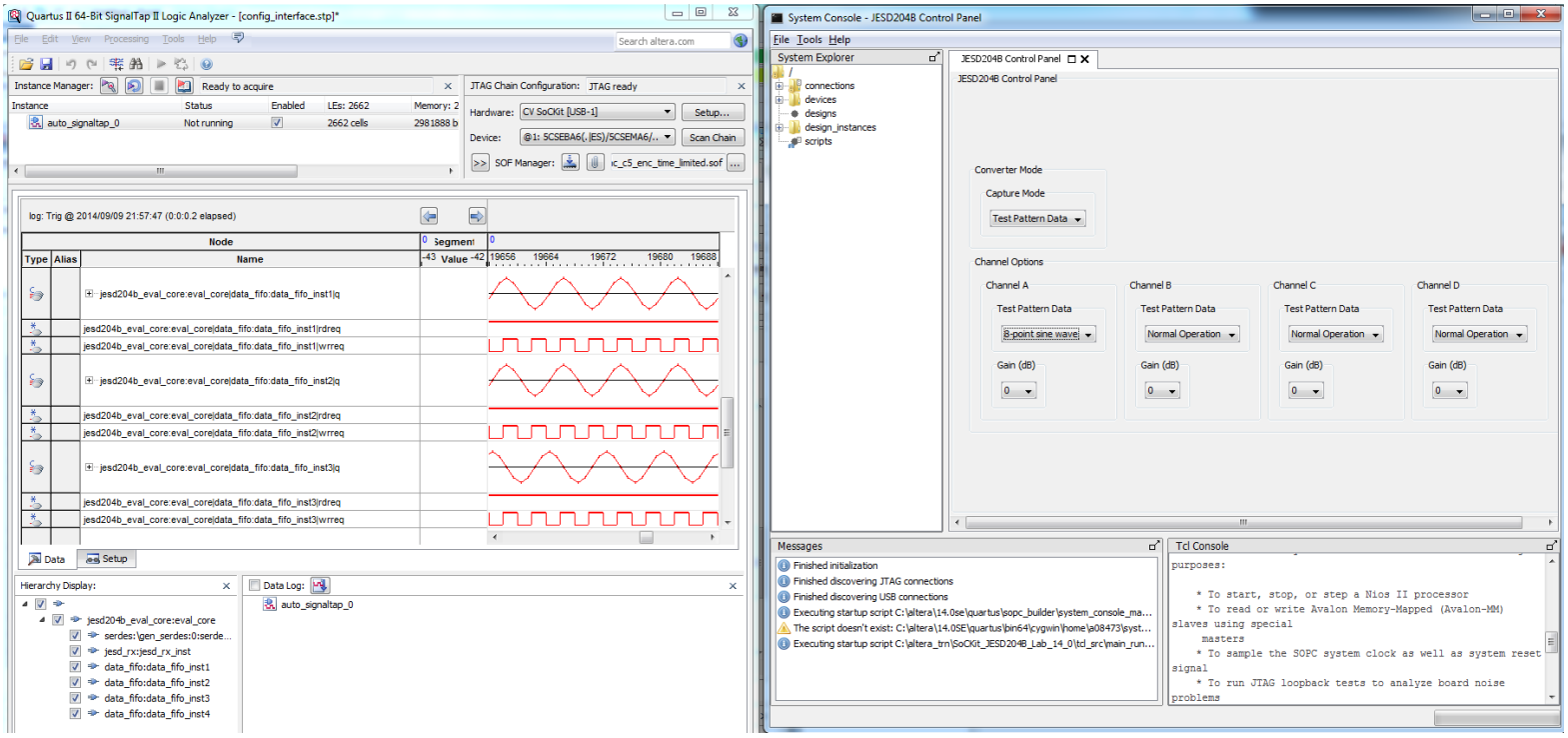
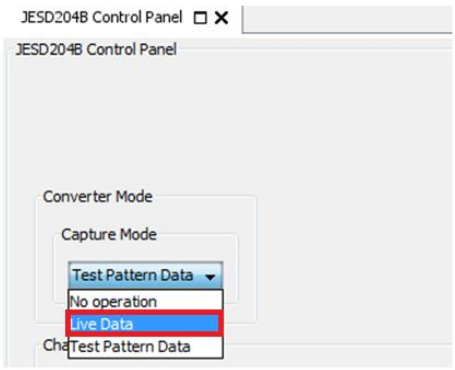
Arrange SignalTap II and System Console in a side by side configuration as shown below.

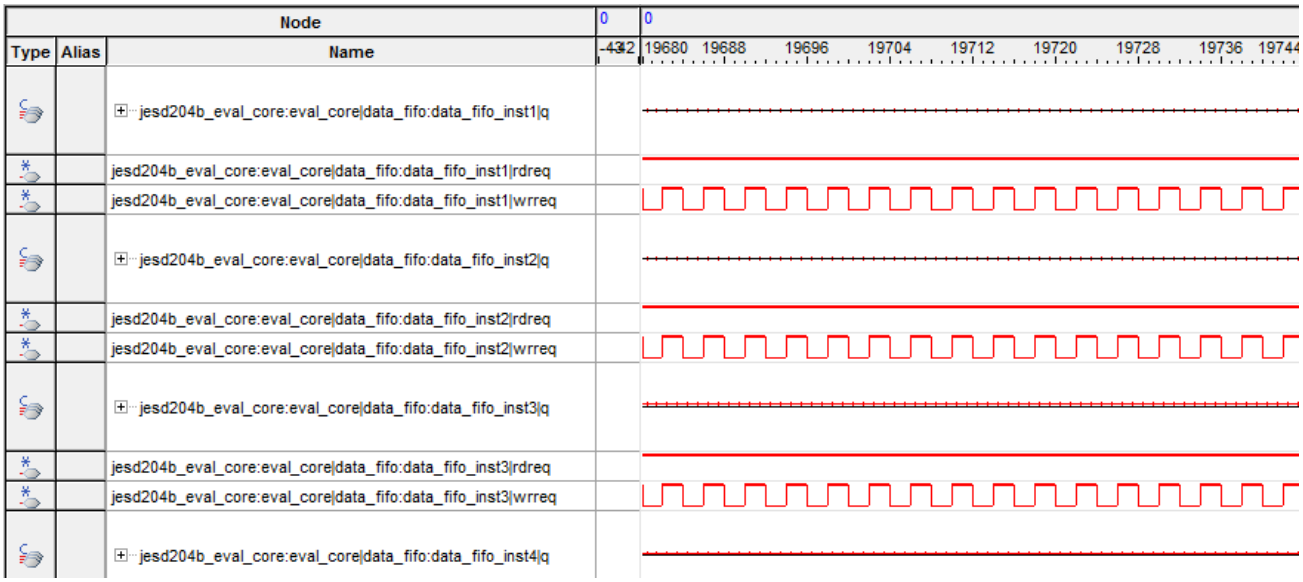


Change the ADC **Capture mode** to Live Data.

- Locate the JESD204B Control Panel in the System Console dashboard.
- Change the Capture Mode to **Live Data**

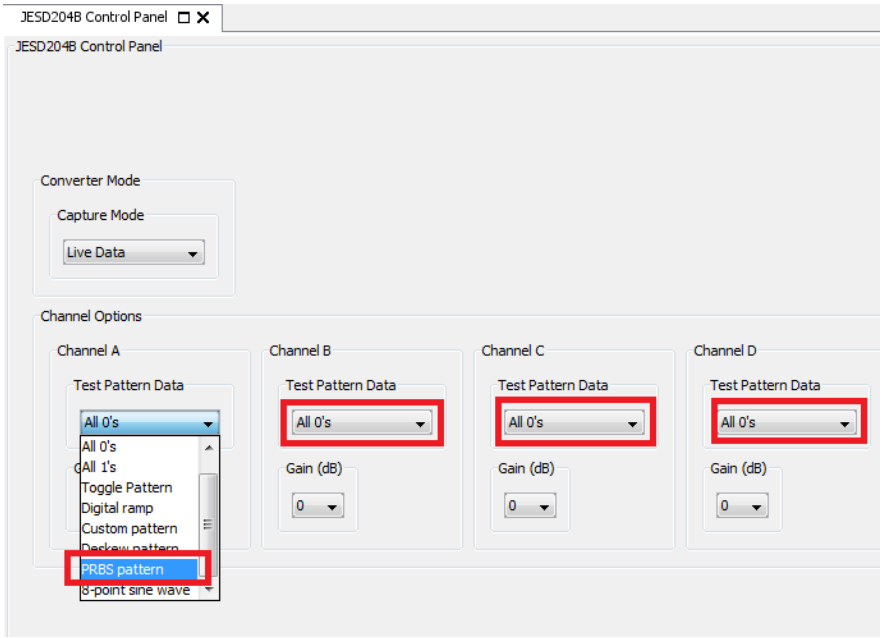


Notice that the 8-point sine wave data has been replaced with zeros. Due to logistical limitations of the lab there is no live data source. The rest of the lab will use the converter in **Test Pattern Mode.**

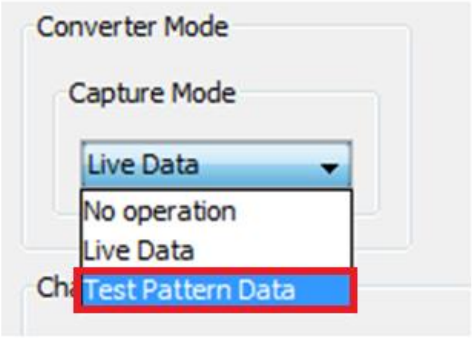


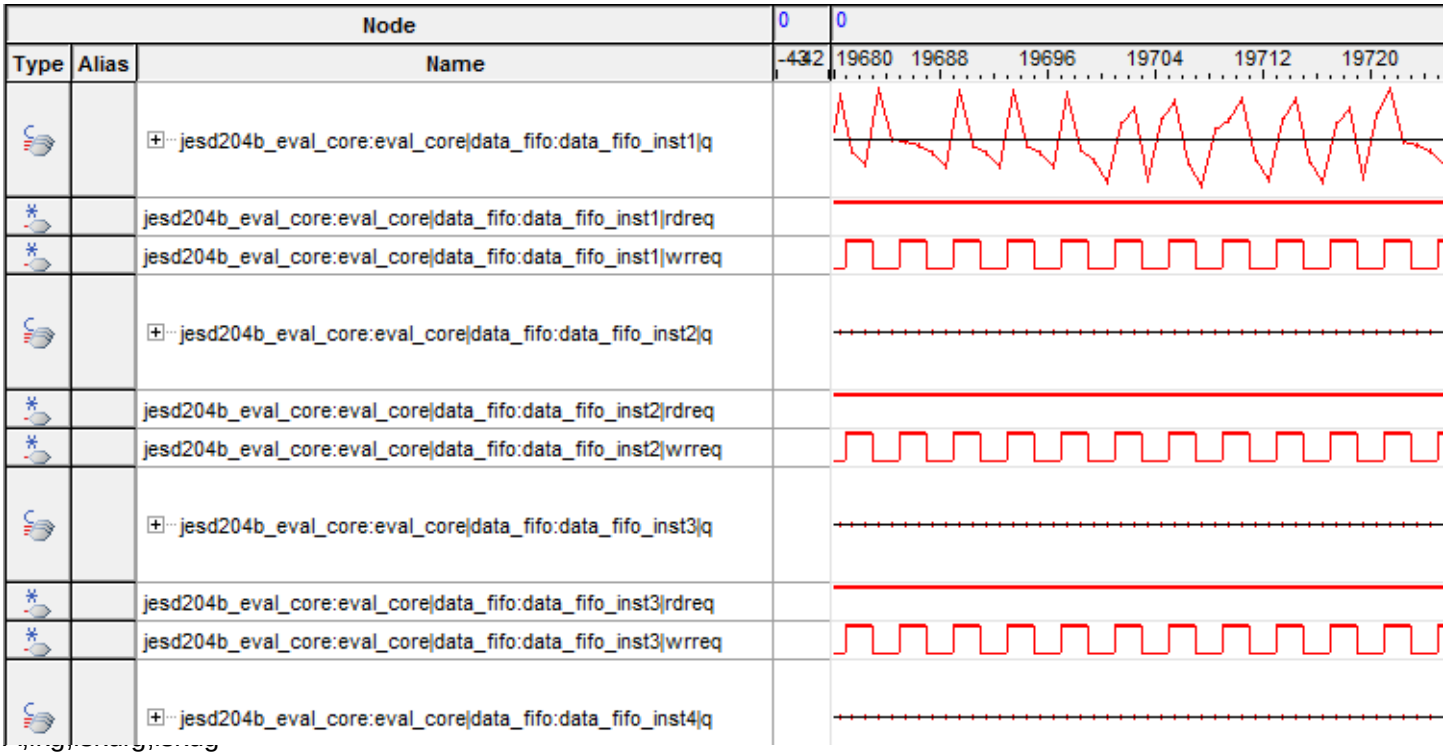
Change the Test Pattern Data options for Channels A through D.

- Use the **pull down** menu option to change **Channel A to PRBS** .
- Change Channels **B through D** to **All 0's**.



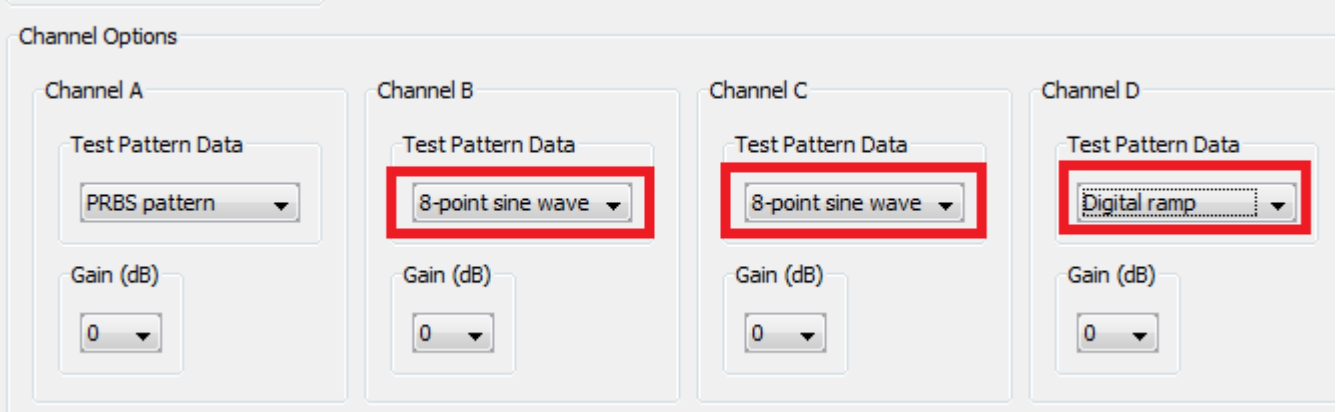
- Change the Capture Mode to **Test Pattern Data**

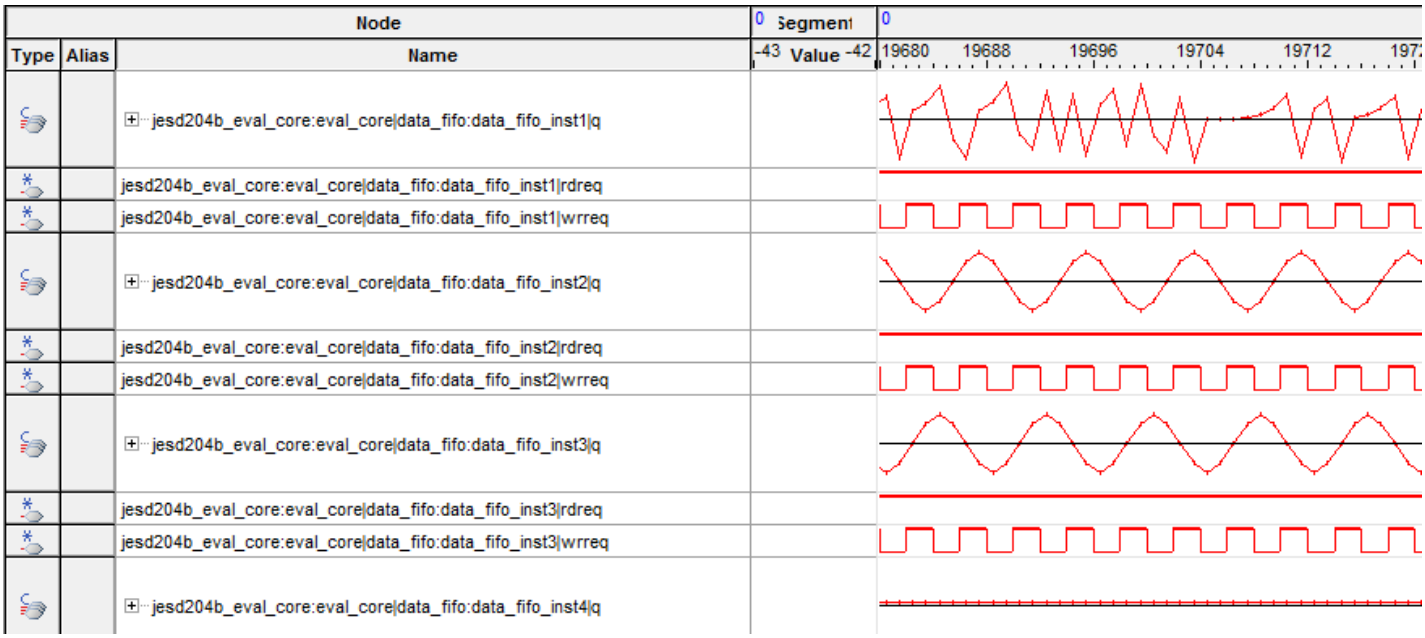




Change the Test Pattern Data options for Channels B through D.

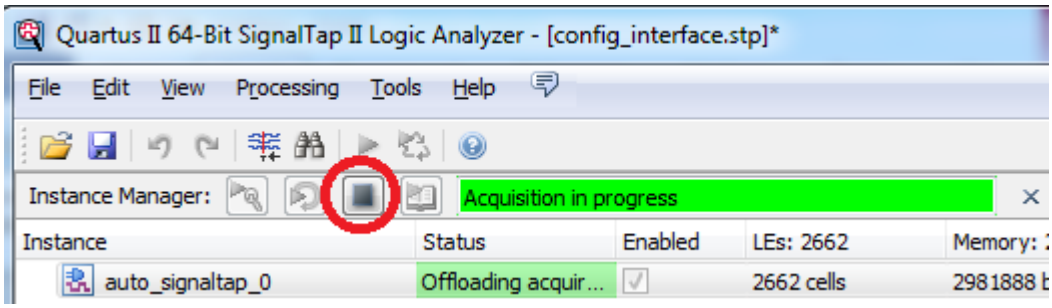
- Use the **pull down** menu option to change **Channel B and C to 8-point sine wave** .
- Change Channels **D to Digital Ramp**.



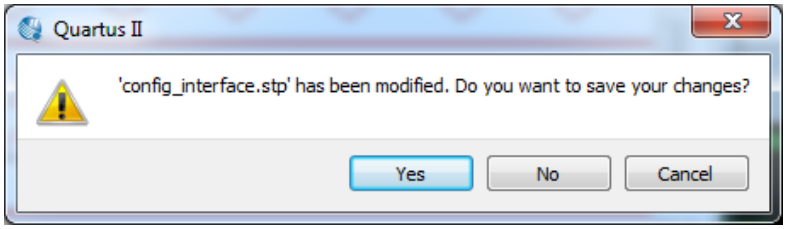


Stop SignalTap II Autorun Analysis and close it

- Press the **Stop Analysis** button
- **File→ Exit**



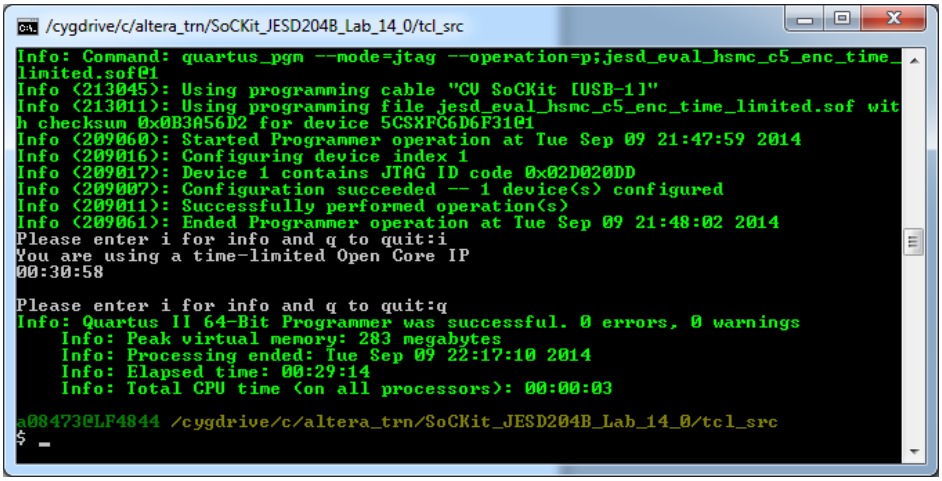
- **Select No** when prompted as shown below



Close System Console

- **File→ Exit**

Press q to exit the Nios II Command Shell script



CONGRATULATIONS!!

You have just successfully captured ADC data using SignalTap II and System Console

MODULE 4. Validation of Acquired Data with High Speed Data Converter Pro

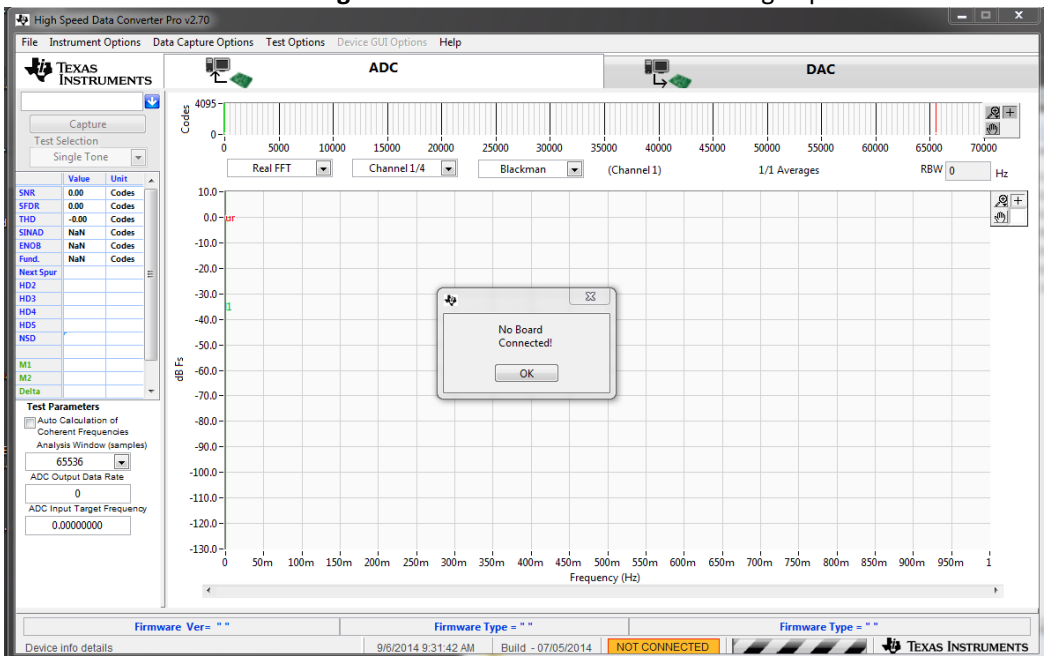
Module Objective

In this module you will utilize HSDC Pro to view acquired data sets for each of the four channels of the ADC34J22, which is a Quad 12-bit 50 MSPS Analog to Digital Converter

4.1 Launch HSDC Pro

- Open High Speed Data Converter Pro

  Select **-> All Programs -> Texas Instruments ->** High Speed Data Converter Pro

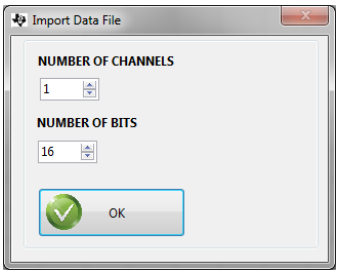


- "No Board Connected!" click "**OK**"

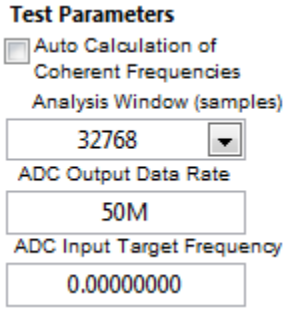
4.2 Analysis of Channel 1 in HSDC Pro

- Import a data file

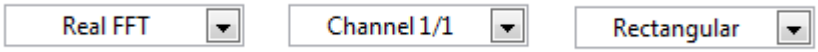
  Select File -> Import Data File and browse to: .. C:\altera_trn\SoCKit_JESD204B_Lab_14_0\ DataFiles \ch1_4_98_p4dbm_32K.txt



- Select “OK”
- Change the ADC Output Data Rate or Sampling Rate to “50M”



- Set the Window type from Blackman to “Rectangular”



- Set the Window type from Blackman to “Rectangular”
- Channel 1 is a transformer coupled channel
- Figure 4.1 shows the SNR for the captured signal at 94.0 dBFs

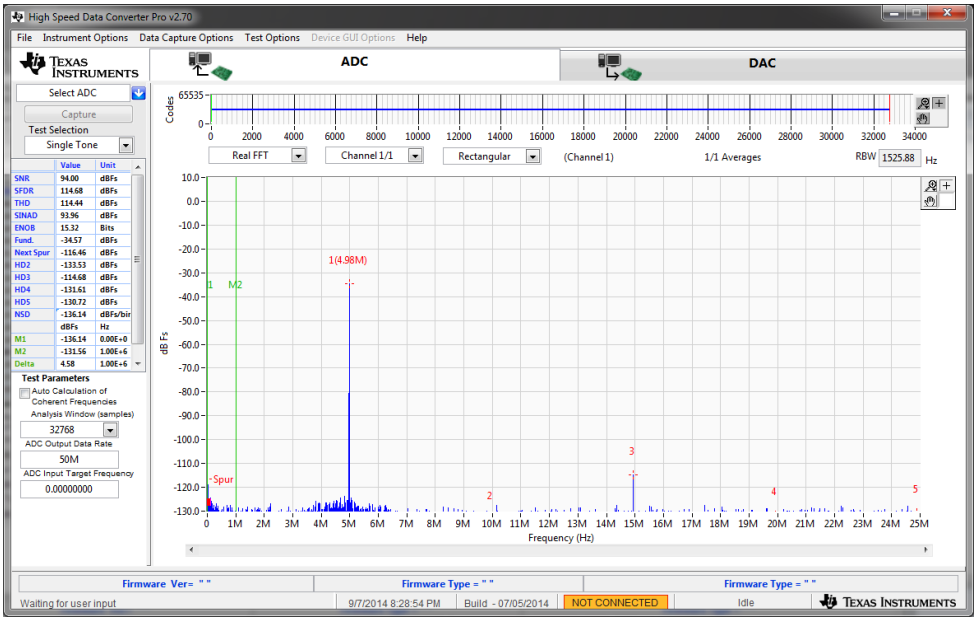
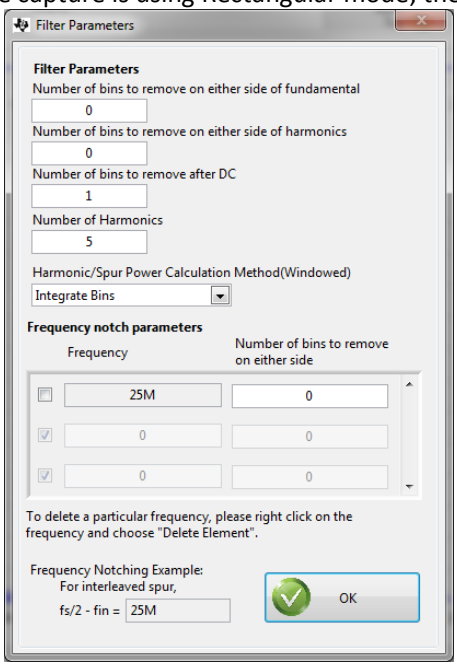


Figure 4.1 ADC43J22 Single Tone FFT Capture Results for Channel 1

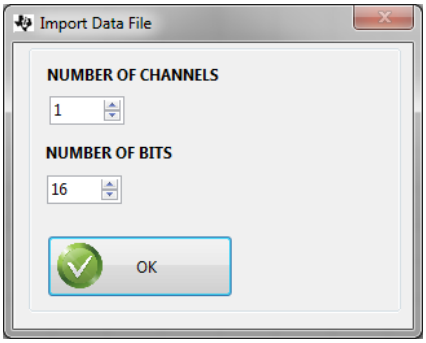
- **Notch Frequency Bins**
  The Notch Frequency Bins option allows the user to remove a number of bins from the SNR calculation of the input frequency around the fundamental, DC and a pre-determined number of harmonics. The default values for these settings when the capture is using Rectangular mode, the default values are 0, 0, 1, 5:



  By default, the noise calculations for SNR and SINAD (Signal-to-noise and distortion ratio) are based on the FFT of the captured data with the Notch Filter parameters applied. The first bin at DC is not used because the first bin contains DC offset and thus does not affect AC parameters or AC performance. The rest of the FFT bins out to the Nyquist frequency are included in the calculation of the total noise.

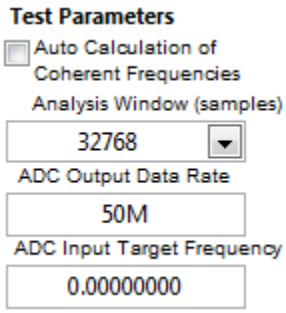
4.3 Analysis of Channel 2 in HSDC Pro

- Import a data file
  Select File -> Import Data File and browse to:
  C:\altera_trn\SoCKit_JESD204B_Lab_14_0\ DataFiles\ ch2_4_98_p4dbm_32K.txt

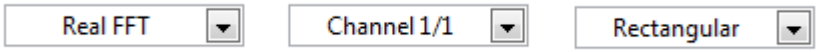


- Select “OK”

- Change the ADC Output Data Rate or Sampling Rate to “50M”



- Set the Window type from Blackman to “Rectangular”



- Set the Window type from Blackman to “Rectangular”
- Channel 2 is a transformer coupled channel
- Figure 4.2 shows the SNR for the captured signal at 94.08 dBFs

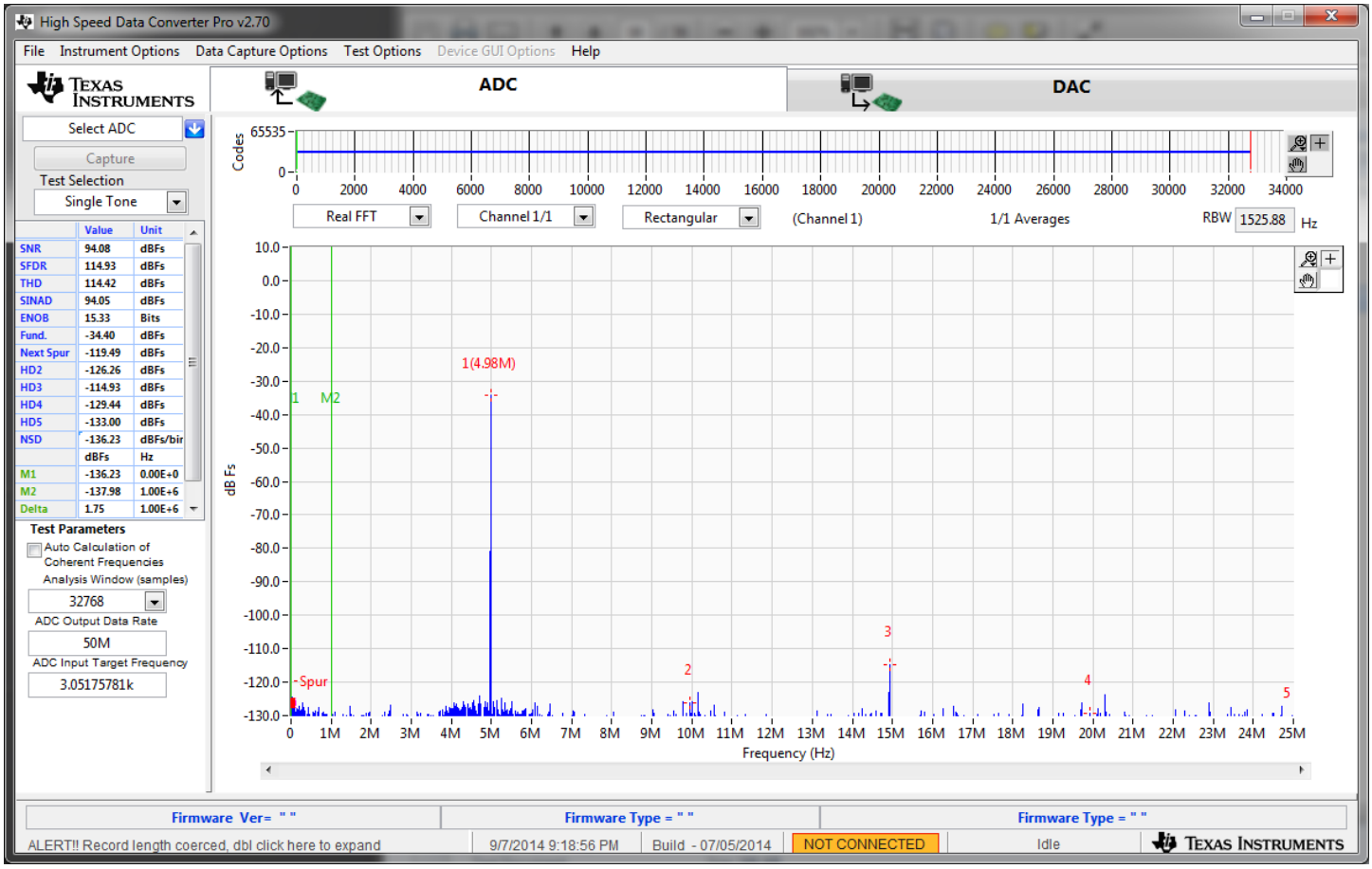
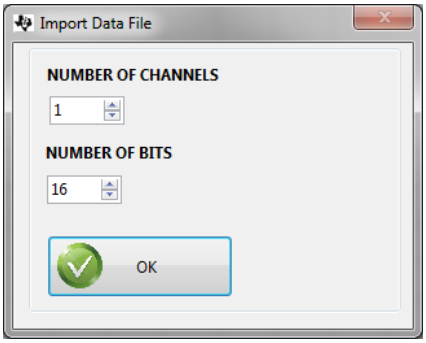


Figure 4.2 ADC43J22 Single Tone FFT Capture Results for Channel 2

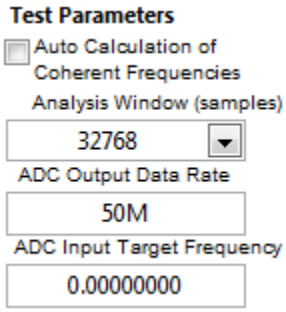
4.4 Analysis of Channel 3 in HSDC Pro

- Import a data file

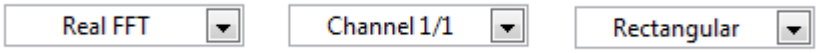
  Select File -> Import Data File and browse to:
  C:\altera_trn\SoCKit_JESD204B_Lab_14_0\DataFiles\ ch3_4_98_m2dbm_32K.txt



- Select “OK”
- Change the ADC Output Data Rate or Sampling Rate to “50M”



- Set the Window type from Blackman to “Rectangular”



- Set the Window type from Blackman to “Rectangular”
- Channel 3 is a directly connected differential channel
- Figure 4.3 shows the SNR for the captured signal at 69.73 dBFs

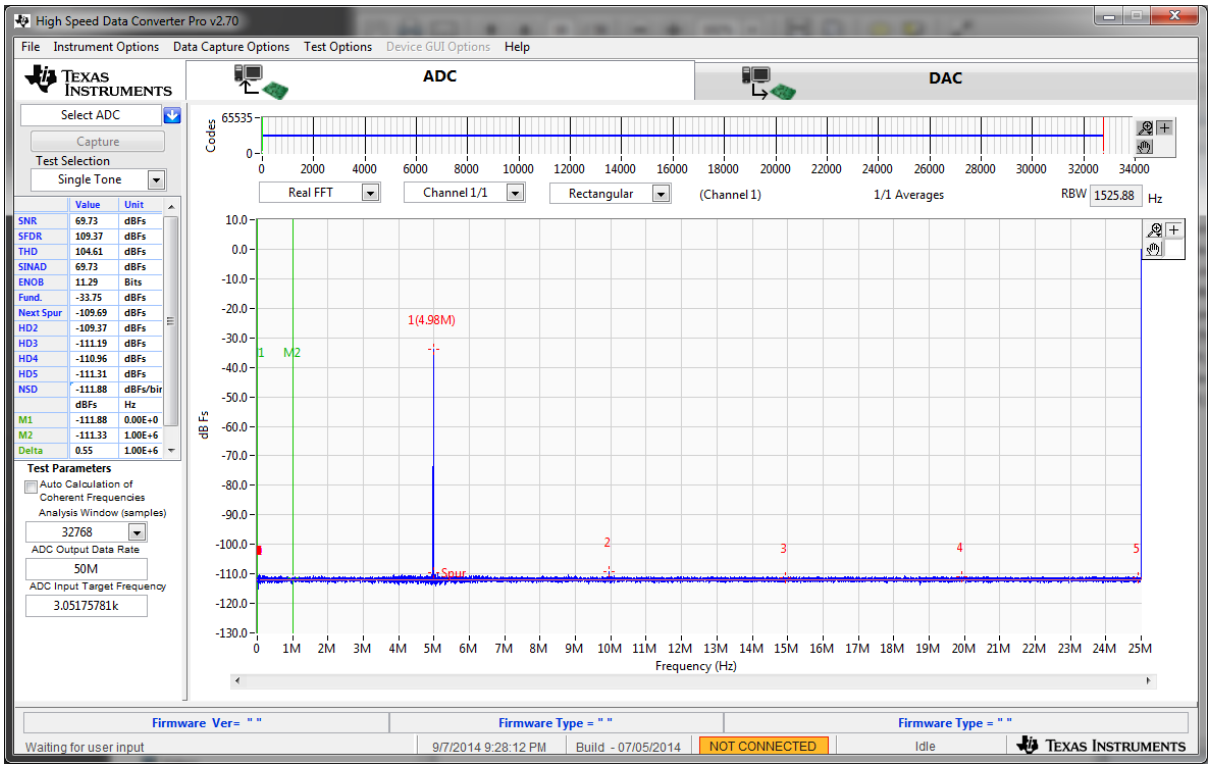


Figure 4.3 ADC43J22 Single Tone FFT Capture Results for Channel 3

CONGRATULATIONS!!

You have completed analyzing your data in HSDC Pro.

MODULE 5. Taking the next Step

Altera has a number of resources available to assist you in further product development at www.altera.com/embedded

Some of the resources available are:

Get more information about the DEV-ADC34J22 from Dallas Logic:

The DEV-ADC34J22 and the Data Sheet
https://parts.arrow.com/item/detail/dallas-logic-corporation/dev-adc34j22#ycp2

An introductory video on the DEV-ADC34J22
https://www.youtube.com/watch?v=QuiRR_F4zUo

Get more information about Qsys:

System Design with Qsys Reference Manual
http://www.altera.com/literature/hb/qts/qsys_intro.pdf

Creating custom Qsys Components
http://www.altera.com/literature/hb/qts/qsys_components.pdf

Visit the rocketboards.org community web site

http://www.rocketboards.org/

Arrow SoCKit Evaluation Board support site
http://www.rocketboards.org/foswiki/Documentation/ArrowSoCKitEvaluationBoard

Altera SoC Development Board support site
http://www.rocketboards.org/foswiki/Documentation/AlteraSoCDevelopmentBoard

Get more information about the SoC HPS

Hard Processor System Technical Reference Manual
http://www.altera.com/literature/hb/cyclone-v/cv_5v4.pdf

Get more information about the SoC Embedded Design Tools

Embedded Software for the Cortex-A9 MPCore Processor
http://www.altera.com/devices/processor/arm/cortex-a9/software/proc-a9-embedded-software.html

Get additional SoC training

Designing with an ARM based SoC
http://www.altera.com/education/training/courses/ISOC101

Developing Software for an ARM based SoC
http://www.altera.com/education/training/courses/ISOC102

For all resources visit www.altera.com/embedded