

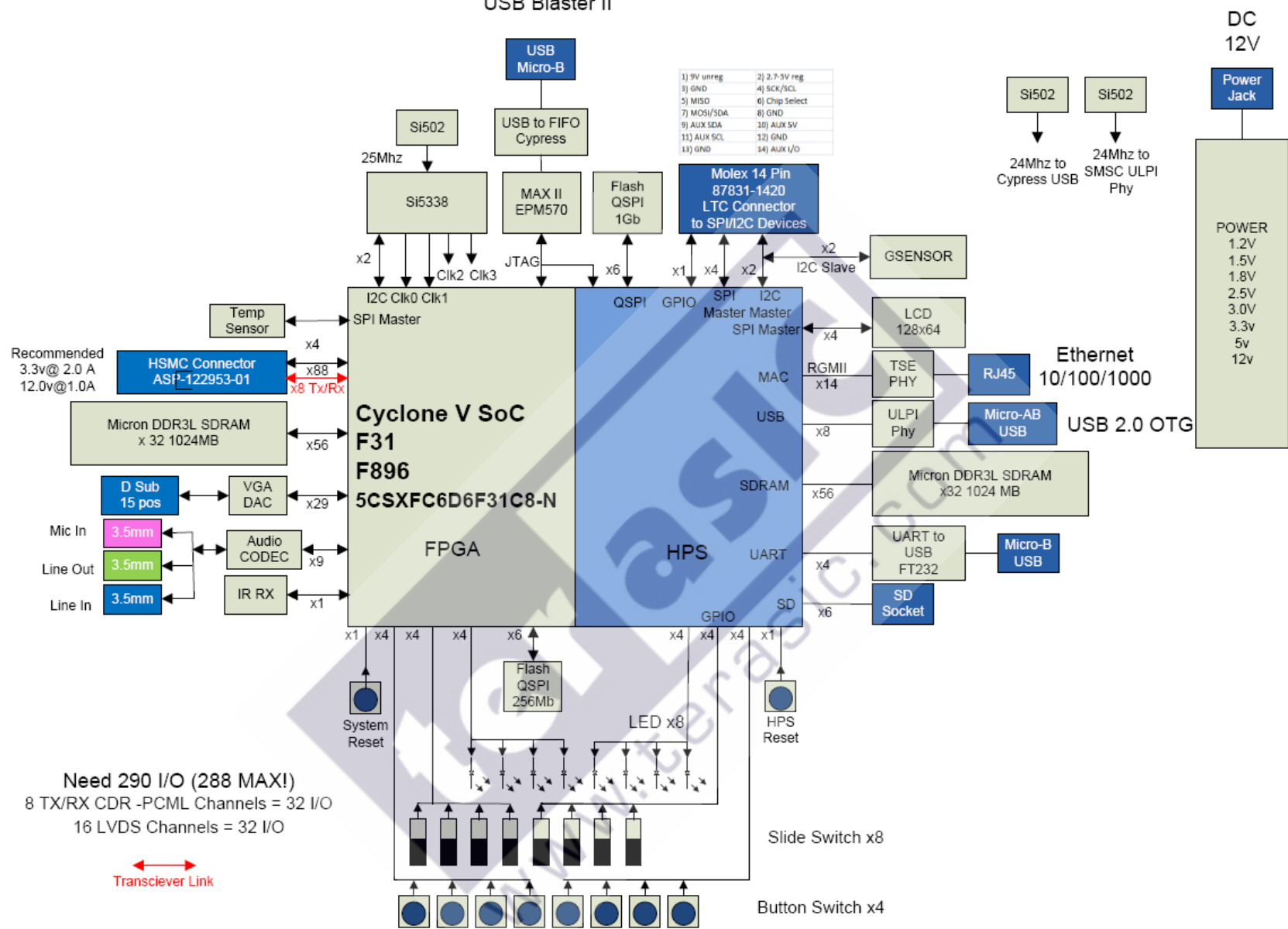
# SoCKit

Section	Title	Page
<b>01.0</b>	<b>Design Introduction</b>	
1.01	Cover Page	1
1.02	Block Diagram	2
<b>02.0</b>	<b>Cyclone V EP5CSXFC6DF31</b>	
02.01	BANK3 & BANK4	3
02.02	BANK5 & BANK6 & BANK8	4
02.03	BANK7	5
02.04	Clock & GND	6
02.05	Transceiver	7
02.06	Config	8
02.07	Power	9
02.08	Decoupling	10
<b>03.0</b>	<b>JTAG</b>	
03.01	USB Blaster II	11
03.02	JTAG Chain	12
<b>04.0</b>	<b>Expansion Port</b>	
04.01	HSMC	13
<b>05.0</b>	<b>Memory</b>	
05.01	DDR3L SDRAM For FPGA	14
05.02	DDR3L SDRAM For HPS	15

Section	Title	Page
<b>06.0</b>	<b>Memory 2</b>	
06.01	QSPI FLASH For FPGA	16
06.02	QSPI FLASH For HPS	17
<b>07.0</b>	<b>LCD &amp; Temp sensor &amp; IRM</b>	
07.01	LCD & Temp sensor & IRM	18
<b>08.0</b>	<b>VGA &amp; Audio</b>	
08.01	VGA ADV7123	19
08.02	Audio SSM2603	20
<b>09.0</b>	<b>FPGA &amp; HPS IO</b>	
09.01	LED & BUTTON & SWITCH For FPGA	21
09.02	LED & BUTTON & SWITCH For HPS	22
<b>10.0</b>	<b>USB &amp; SD CARD &amp; UART</b>	
10.01	UART TO USB & SD CARD	23
10.02	ULPI PHY USB3300	24
<b>11.0</b>	<b>TSE PHY</b>	
11.01	TSE PHY KSZ9021RN	25
<b>12.0</b>	<b>LTC Connector &amp; G Sensor</b>	
12.01	LTC Connector & G Sensor	26

Section	Title	Page
<b>13.0</b>	<b>ADC &amp; DAC</b>	
13.01	Soft ADC & DAC	27
<b>14.0</b>	<b>System Power</b>	
14.01	9V & 5V	28
14.02	1.1V & 1.2V	29
14.03	3.3V & 2.5V	30
14.04	1.5V	31
14.05	HSMC_VCCIO	32

# USB Blaster II



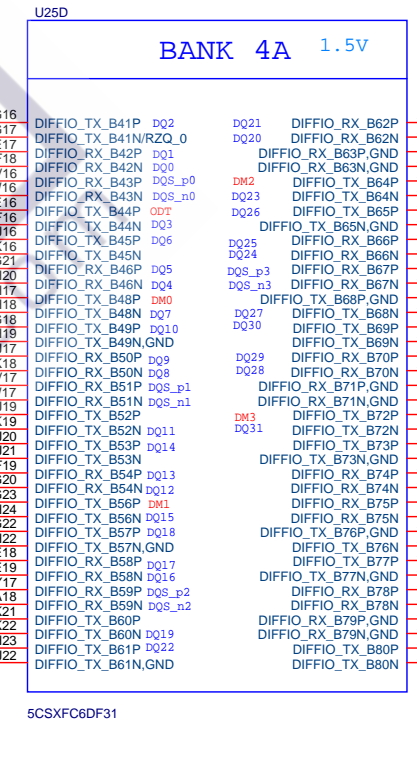
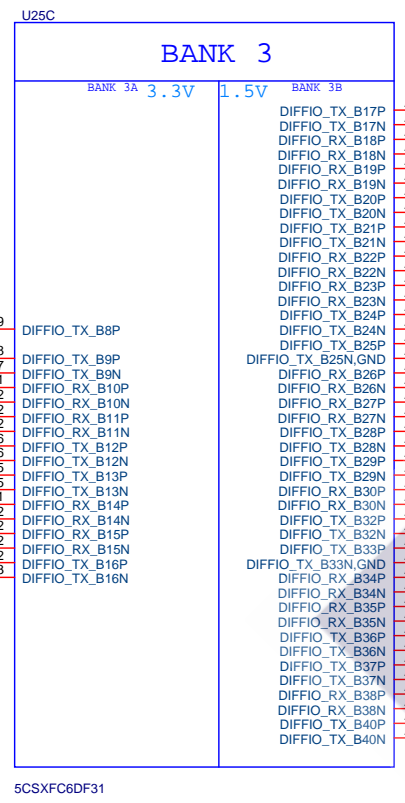
VGA\_R[7..0] 19

11 USB B2\_CLK  
 11 USB RESET\_n  
 11 USB OE\_n  
 11 USB RD\_n  
 11 USB WR\_n  
 11 USB SCL  
 11 USB FULL  
 11 USB EMPTY  
 11 USB\_SDA

11 USB\_B2\_DATA[7..0]

14 FPGA\_DDR3\_CK\_p  
 14 FPGA\_DDR3\_CK\_n  
 14 FPGA\_DDR3\_CKE  
 14 FPGA\_DDR3\_RESET\_n  
 14 FPGA\_DDR3\_WE\_n  
 14 FPGA\_DDR3\_RAS\_n  
 14 FPGA\_DDR3\_CAS\_n  
 14 FPGA\_DDR3\_CS\_n  
 14 FPGA\_DDR3\_ODT

FPGA\_DDR3\_A[14..0]  
 FPGA\_DDR3\_DM[3..0]  
 FPGA\_DDR3\_BA[2..0]  
 FPGA\_DDR3\_DQ[31..0]  
 FPGA\_DDR3\_DQS\_p[3..0]  
 FPGA\_DDR3\_DQS\_n[3..0]



18 TEMP\_SCLK AF9

18 TEMP\_CS\_n AF8

18 TEMP\_DIN AG7

18 TEMP\_DOUT AG1

18 IRDA\_RXD AH2

VGA\_R1 AA12

VGA\_R2 AB12

VGA\_R3 AF6

VGA\_R4 AG6

VGA\_R0 AG5

VGA\_R6 AH5

VGA\_R7 AJ1

VGA\_R5 AJ2

VGA\_VS AC12

VGA\_HS AD12

VGA\_SYNC\_n AG2

VGA\_BLANK\_n AH3

R265 100

FPGA\_DDR3\_DQ2 AG16

FPGA\_DDR3\_RZQ0 AG17

FPGA\_DDR3\_DQ1 AE17

FPGA\_DDR3\_DQ0 AF18

FPGA\_DDR3\_DQS\_p0 V16

FPGA\_DDR3\_DQS\_n0 W16

FPGA\_DDR3\_ODT AE16

FPGA\_DDR3\_DQ3 AF16

FPGA\_DDR3\_DQ6 AJ16

FPGA\_DDR3\_DQ5 AK16

FPGA\_DDR3\_DQ4 AH20

FPGA\_DDR3\_DM0 AH17

FPGA\_DDR3\_DQ7 AH18

FPGA\_DDR3\_DQ10 AG18

FPGA\_DDR3\_DQ11 AH19

FPGA\_DDR3\_DQ9 AK17

FPGA\_DDR3\_DQ8 AK18

FPGA\_DDR3\_DQS\_p1 V17

FPGA\_DDR3\_DQS\_n1 W17

FPGA\_DDR3\_DQ11 AK19

FPGA\_DDR3\_DQ14 AJ20

FPGA\_DDR3\_CKE AJ21

FPGA\_DDR3\_DQ13 AF19

FPGA\_DDR3\_DQ12 AG20

FPGA\_DDR3\_DM1 AG23

FPGA\_DDR3\_DQ15 AH24

FPGA\_DDR3\_DQ18 AG22

FPGA\_DDR3\_DQ17 AE18

FPGA\_DDR3\_DQ16 AE19

FPGA\_DDR3\_DQS\_p2 Y17

FPGA\_DDR3\_DQS\_n2 Y18

FPGA\_DDR3\_RESET\_n AK21

FPGA\_DDR3\_DQ19 AK22

FPGA\_DDR3\_DQ22 AH23

AJ22

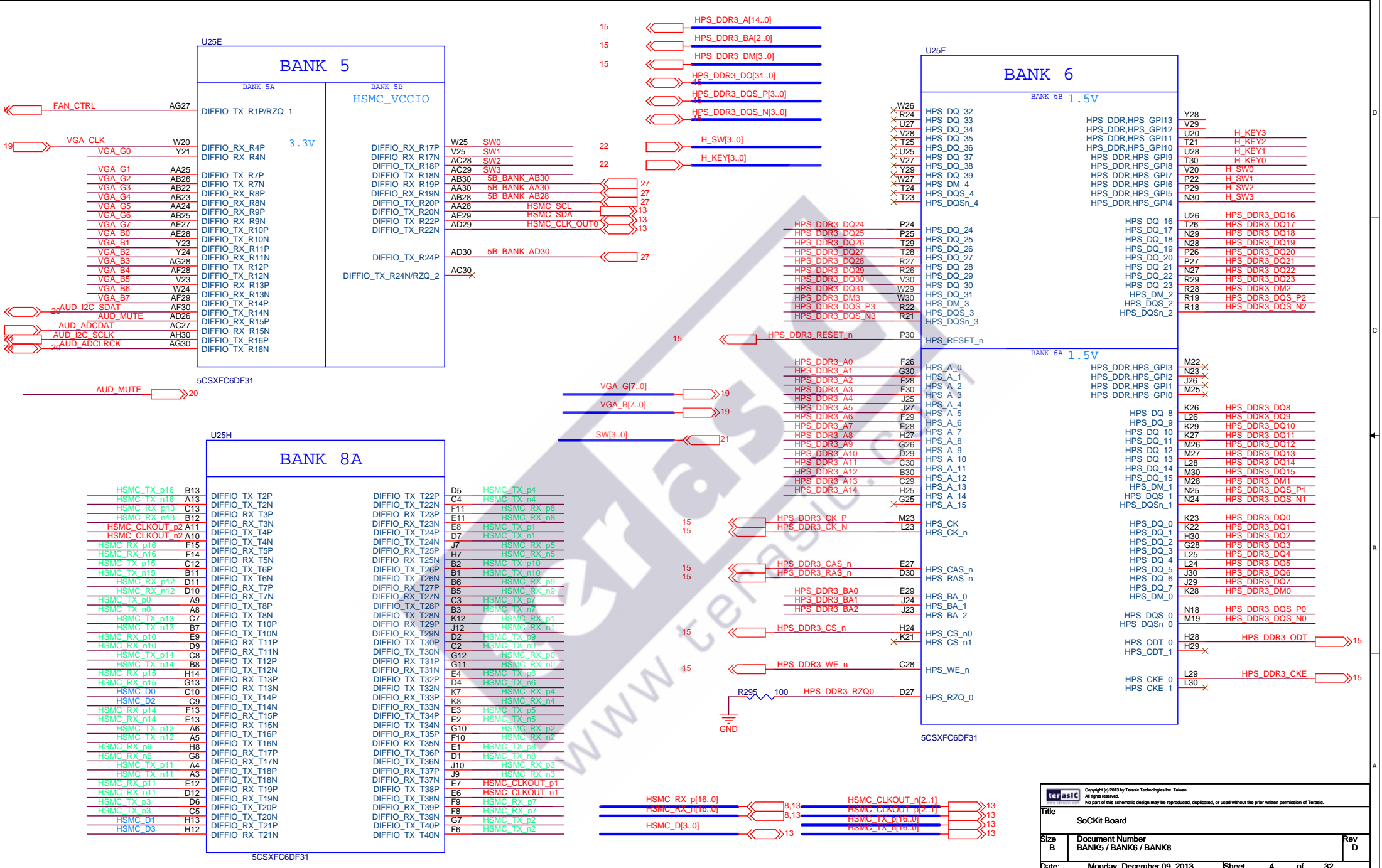
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

**terasic**

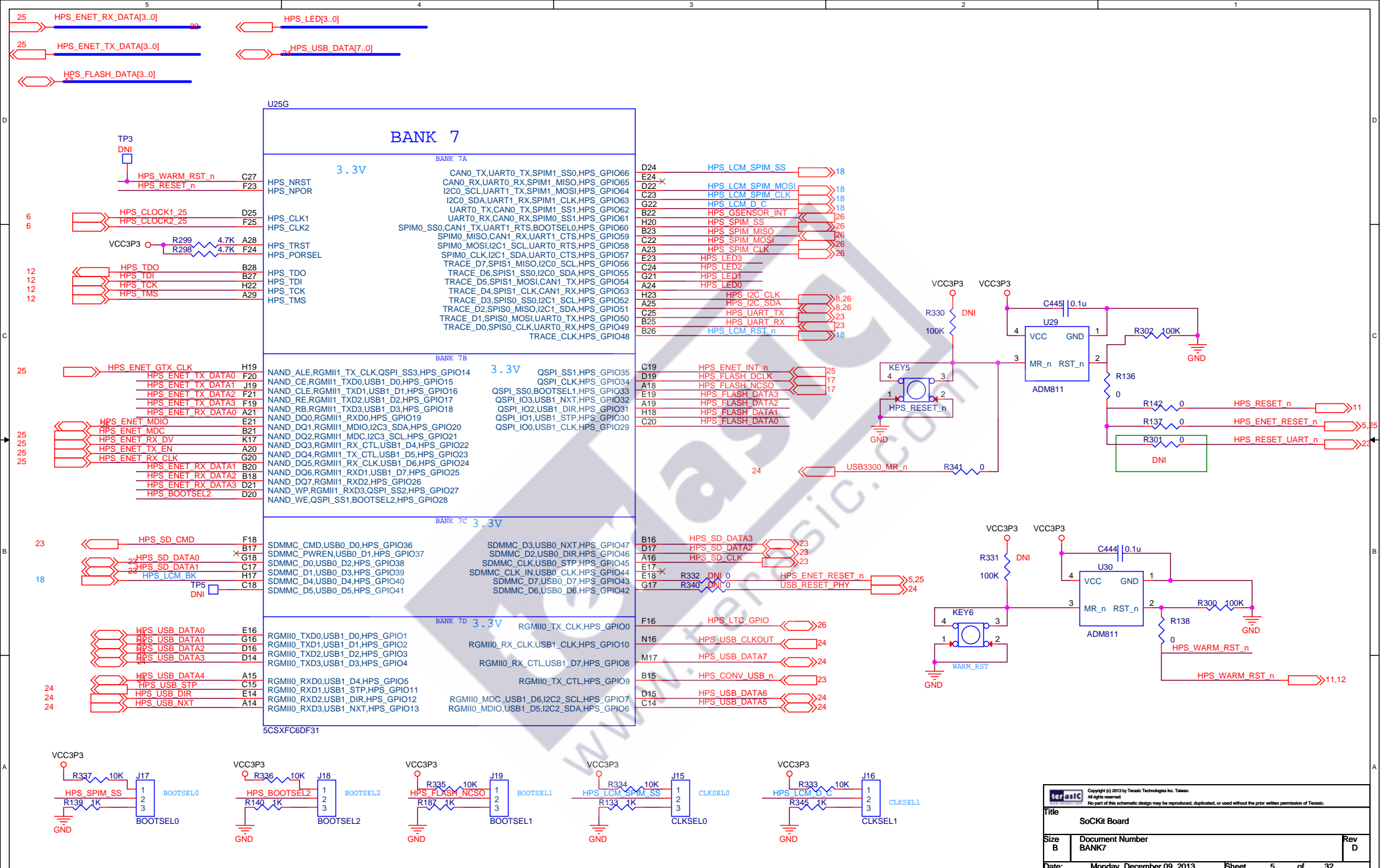
Title: SoCKit Board

Size: B Document Number: BANK3 & BANK4 Rev: D

Date: Monday, December 09, 2013 Sheet: 3 of 32

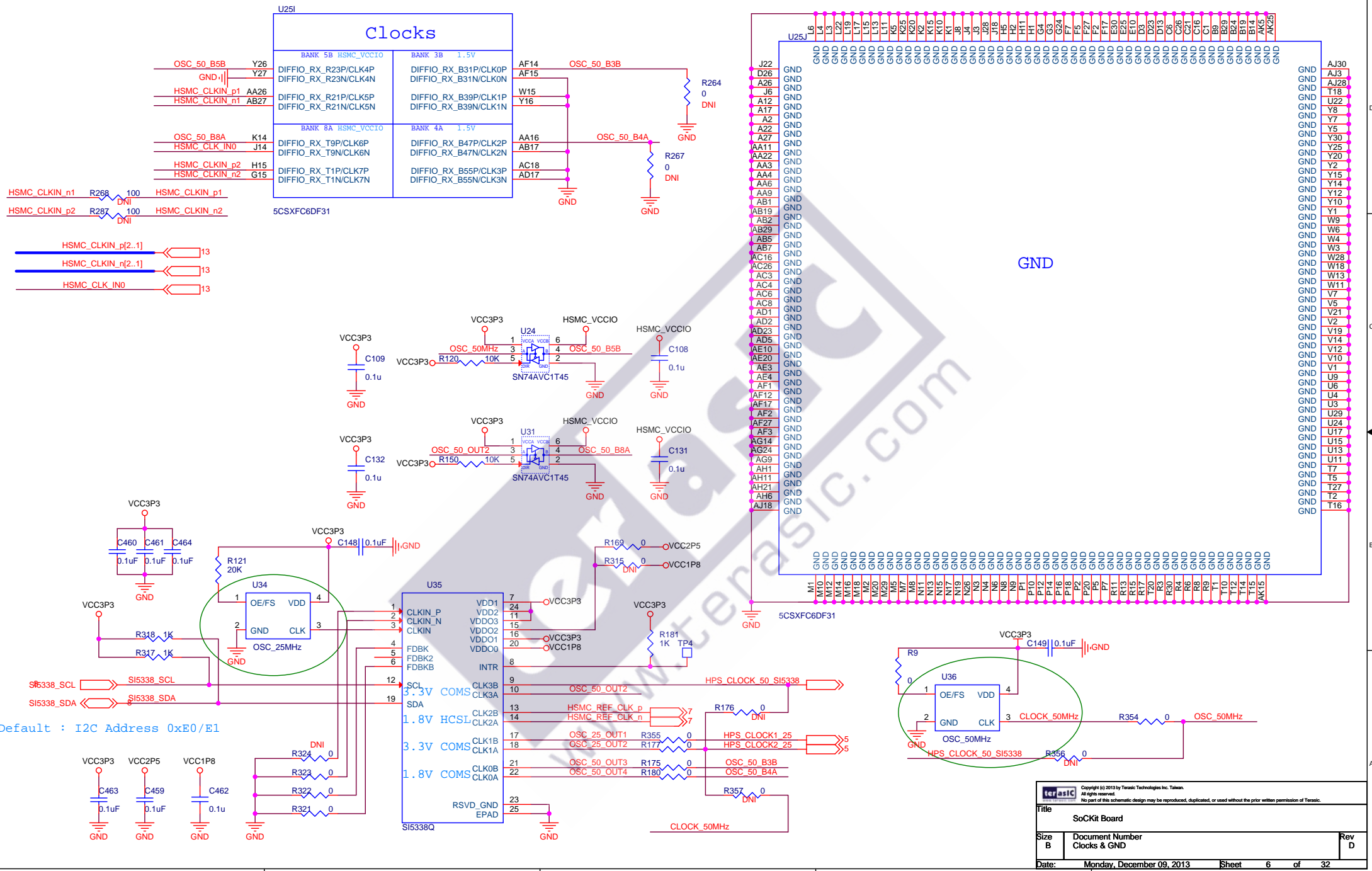


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title: SoCKit Board		
Size B	Document Number: BANK5 / BANK6 / BANK8	Rev D
Date:	Monday, December 09, 2013	Sheet 4 of 32

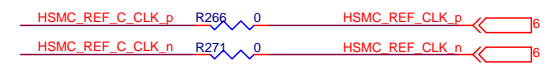
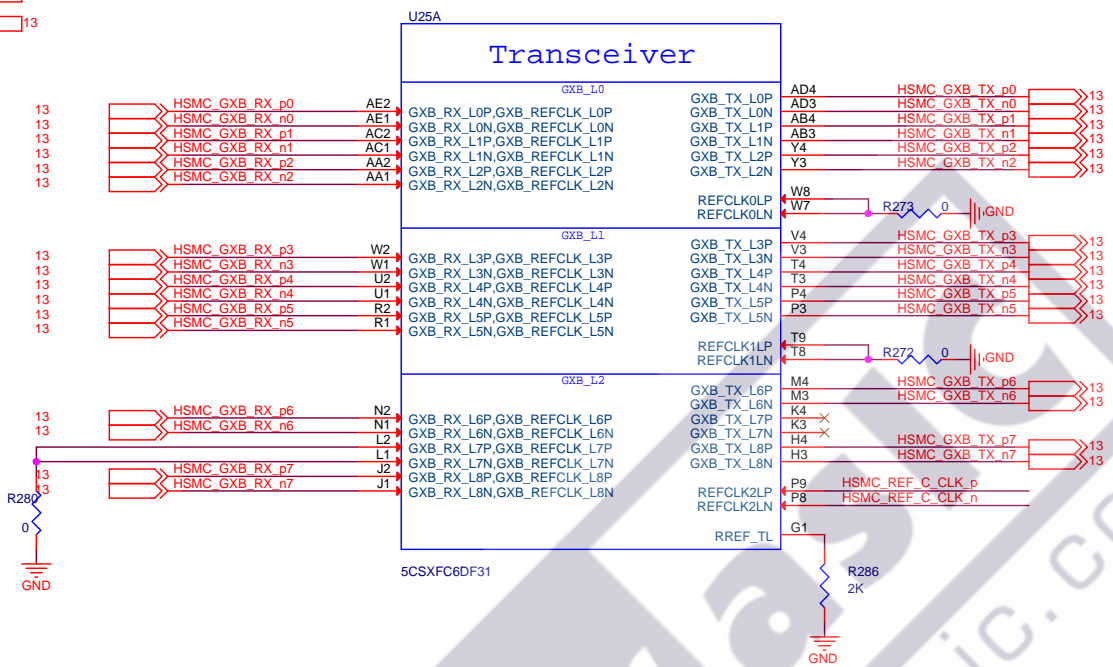
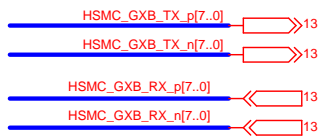


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
SoCKit Board		
Size	Document Number	Rev
B	BANK7	D
Date:	Monday, December 09, 2013	Sheet 5 of 32

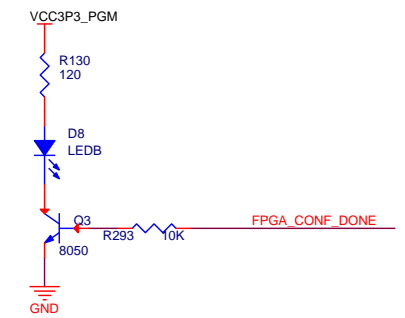
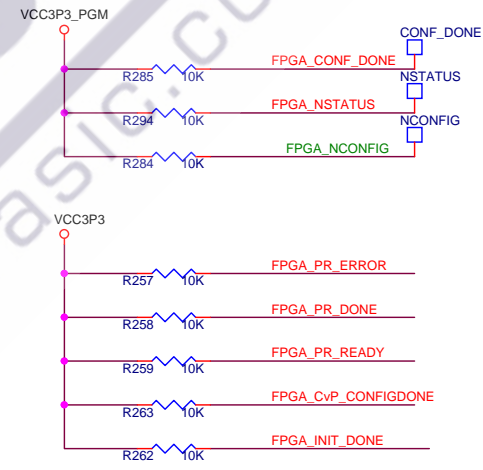
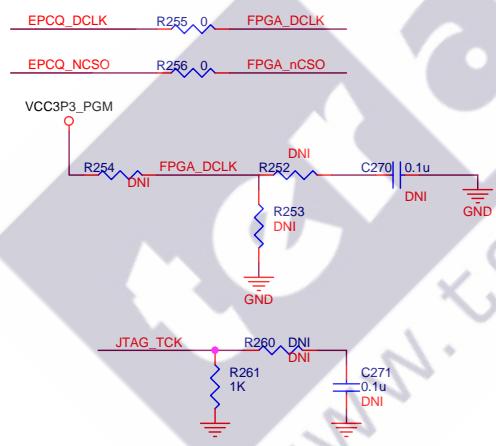
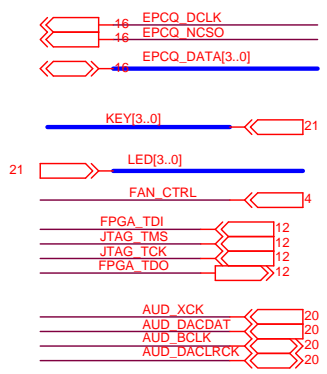
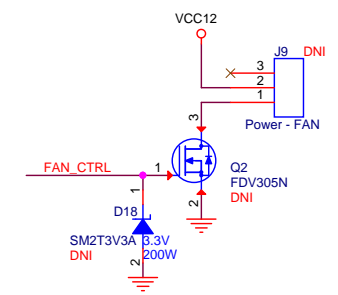
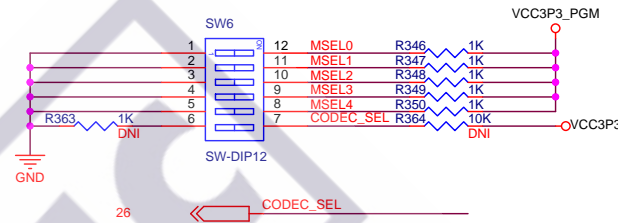
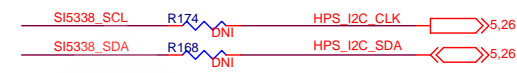
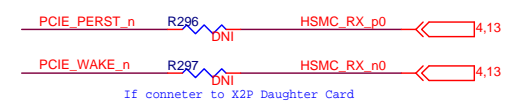
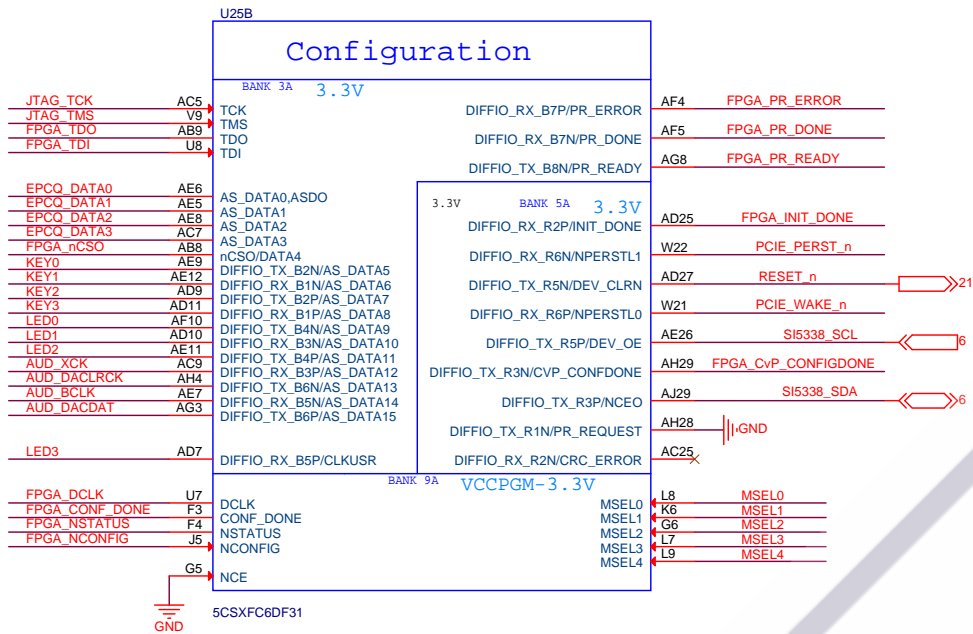





		Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.
Title		
SoCKit Board		
Size	Document Number	Rev
B	Clocks & GND	D
Date: Monday, December 09, 2013		Sheet 6 of 32

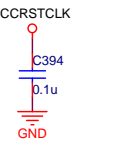
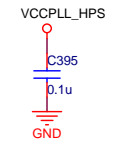
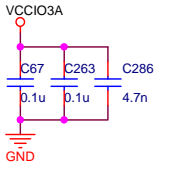
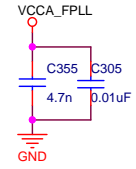
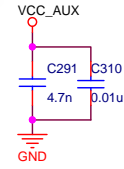
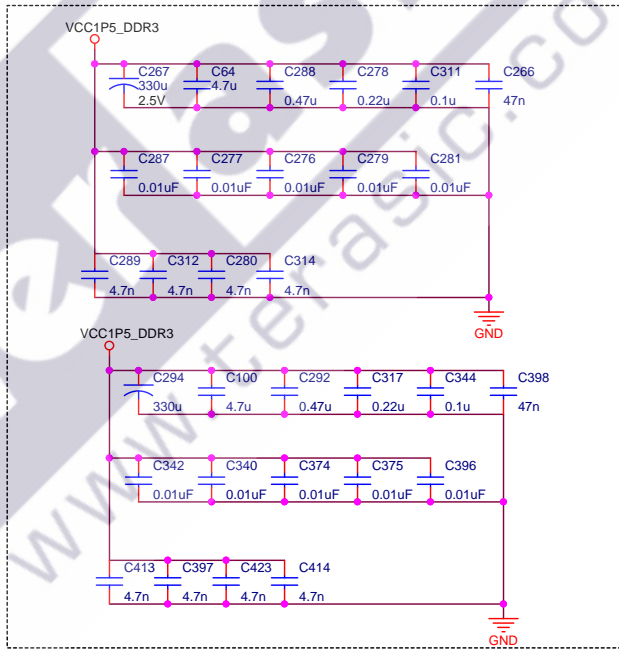
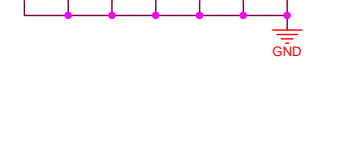
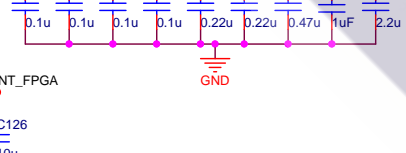
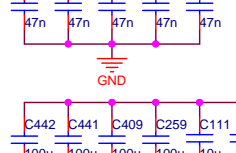
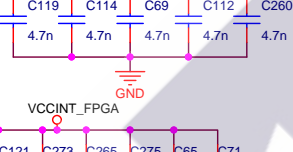
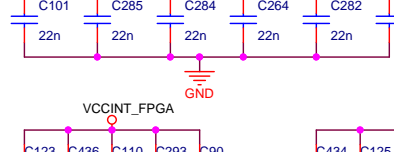
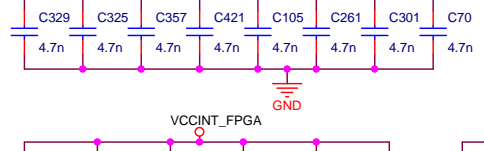
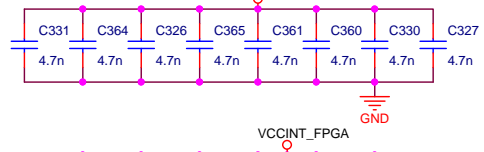
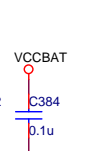
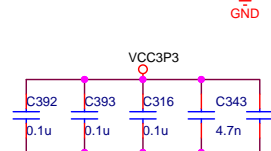
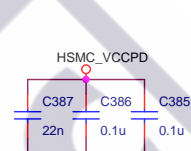
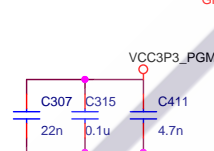
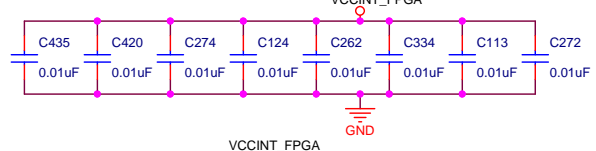
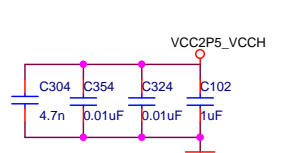
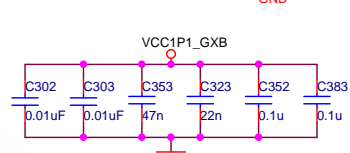
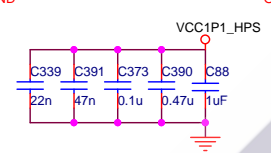
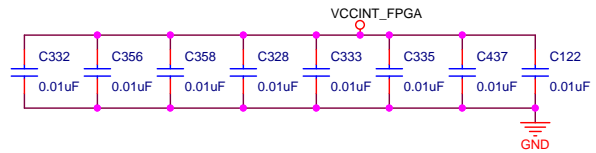
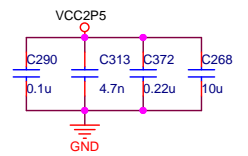
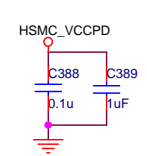
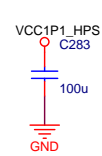
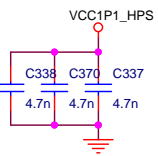
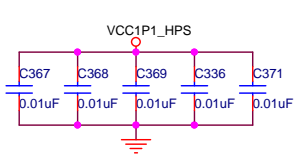
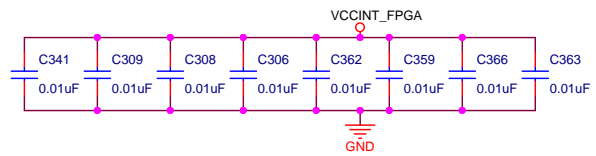


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title: SoCKit Board		
Size: B	Document Number: Transceiver	Rev: D
Date: Monday, December 09, 2013	Sheet: 7	of 32



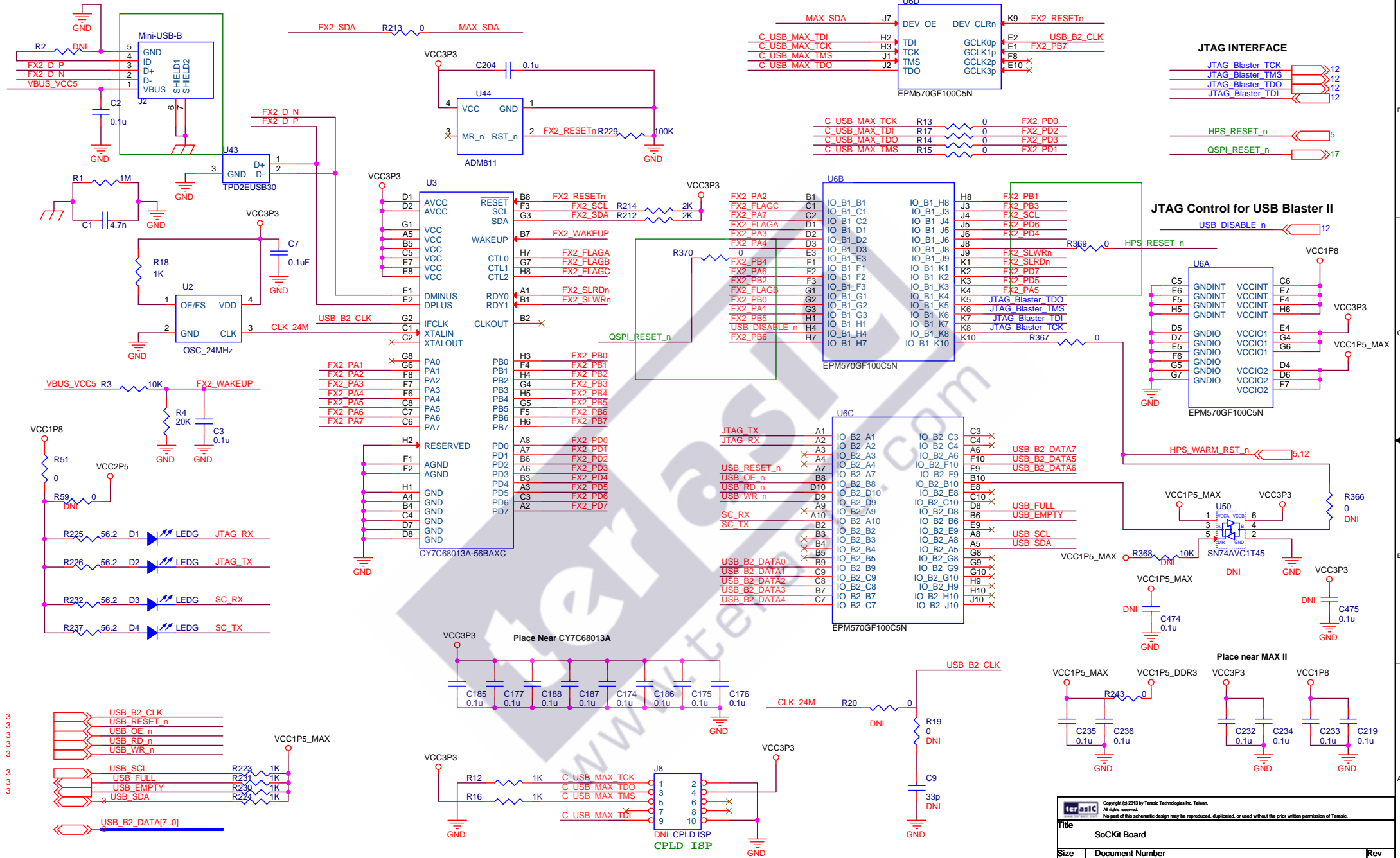
 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
SoCKit Board		
Size	Document Number	Rev
B	Config	D
Date:	Monday, December 09, 2013	Sheet 8 of 32





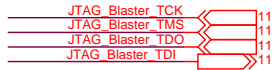
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title: SoCKit Board		
Size B	Document Number: Decoupling	Rev D
Date: Monday, December 09, 2013	Sheet 9	of 32



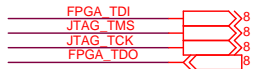


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
SoCKit Board		
Size B	Document Number	Rev D
USB Blaster II		
Date:	Monday, December 09, 2013	Sheet 11 of 32

**USB Blaster**



**FPGA JTAG INTERFACE**



**HSMC JTAG INTERFACE**

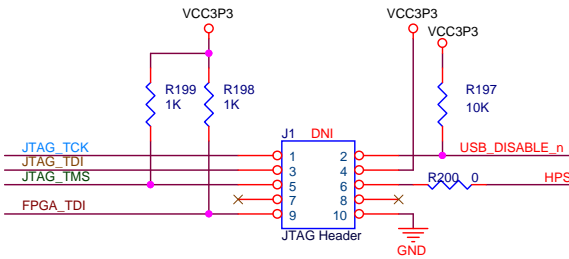


**HPS JTAG INTERFACE**

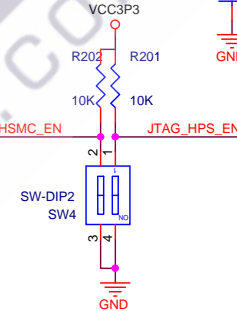
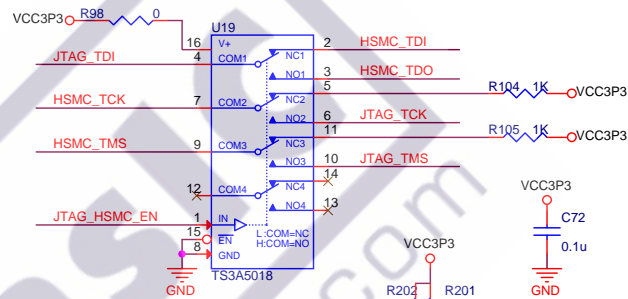
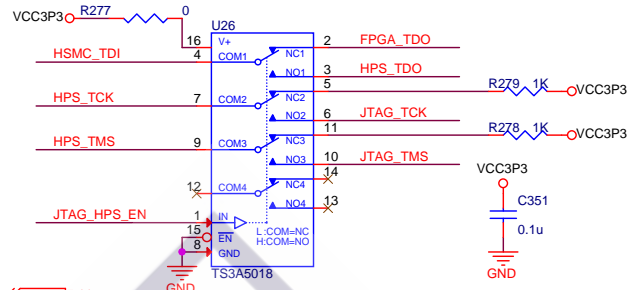


FPGA\_TDO R123 0 HPS\_TDI 5,12

JTAG\_Blaster\_TDO R71 0 FPGA\_TDI  
 JTAG\_Blaster\_TMS R72 0 JTAG\_TMS  
 JTAG\_Blaster\_TCK R74 0 JTAG\_TCK  
 JTAG\_Blaster\_TDI R73 0 JTAG\_TDI



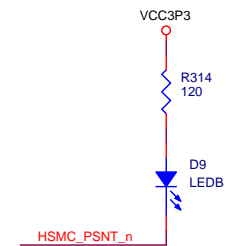
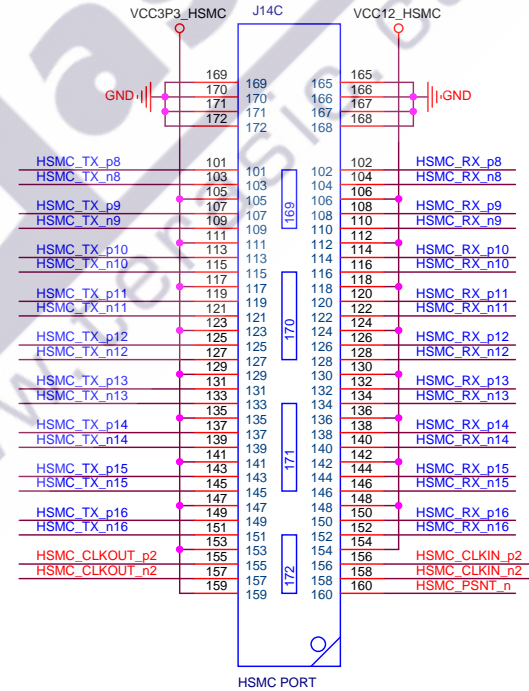
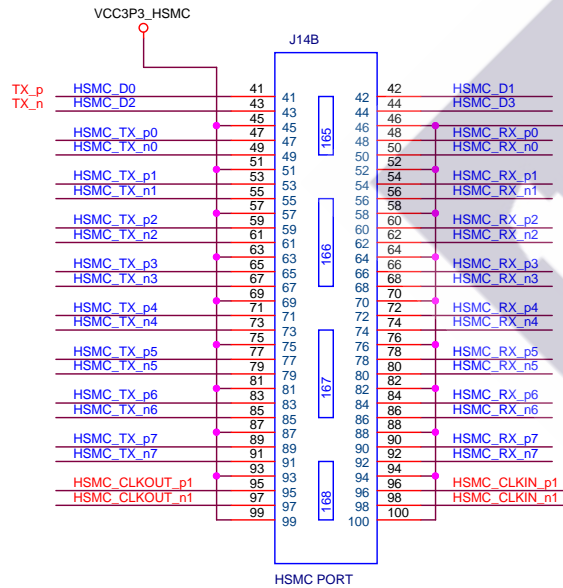
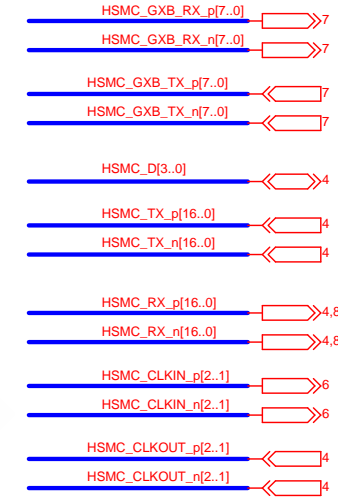
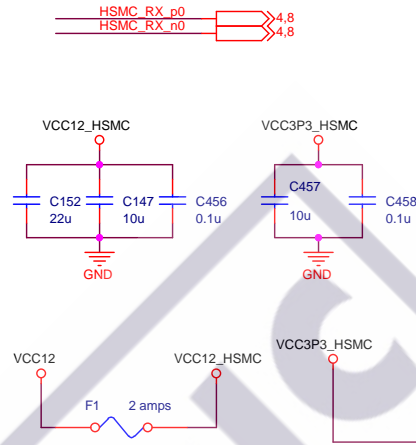
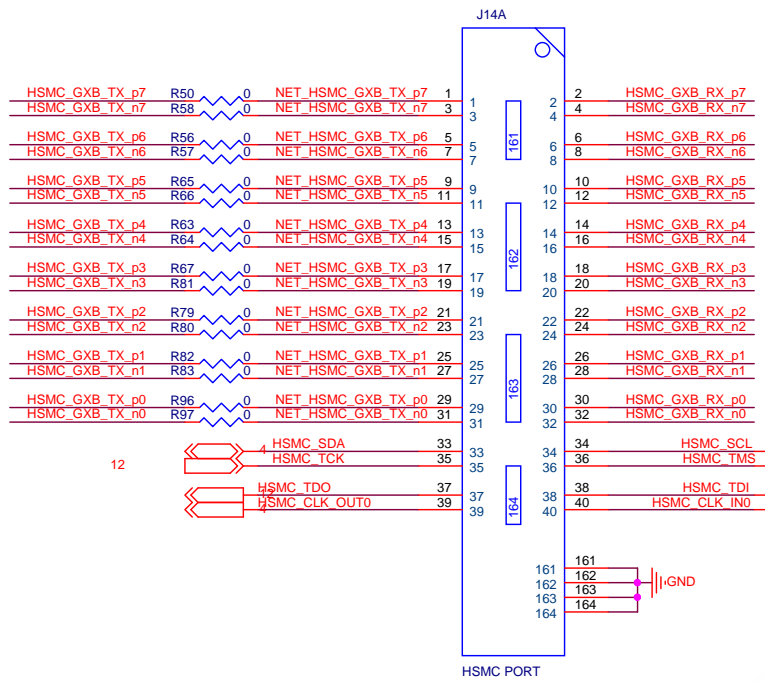
USB\_DISABLE\_n 11



**Default Disable (switch OFF)**

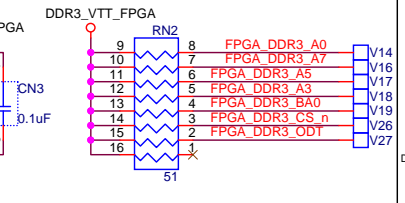
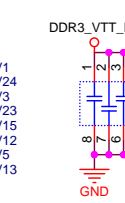
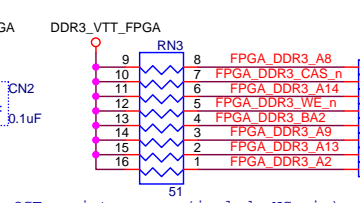
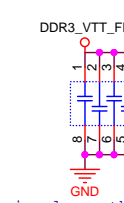
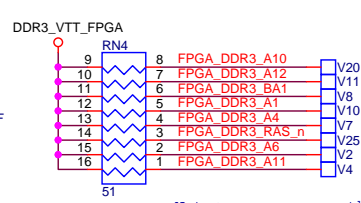
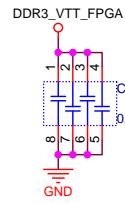
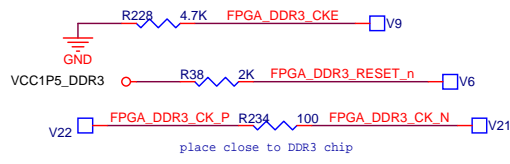
OFF = in-chain  
 ON = not-in-chain

Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
SoCKit Board		
Size	Document Number	Rev
B	JTAG Chain	D
Date:	Monday, December 09, 2013	Sheet 12 of 32

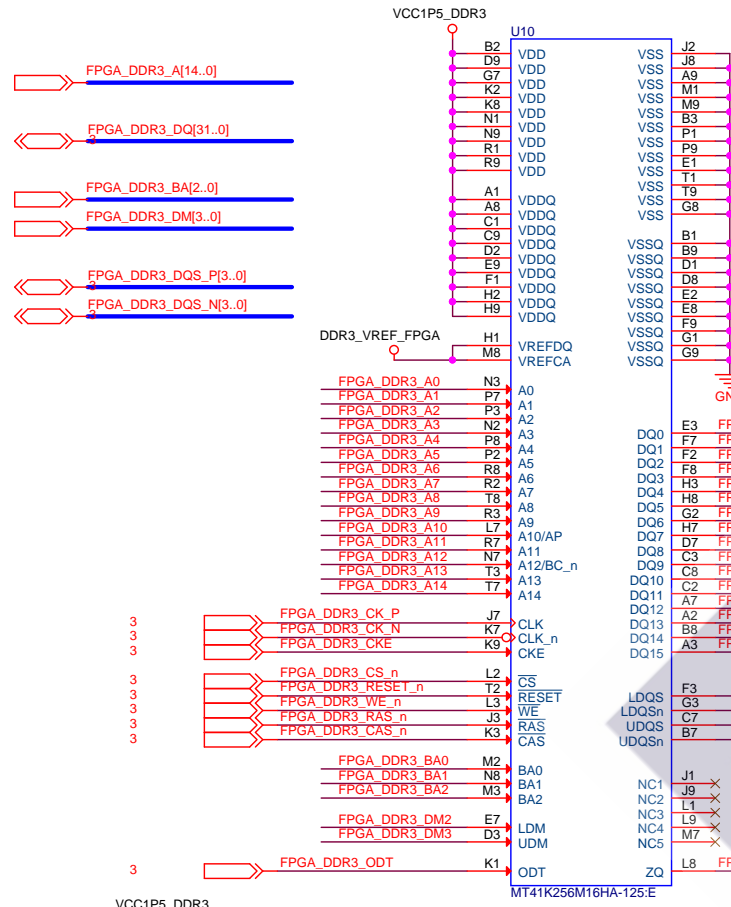


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title: SoCKit Board		
Size: B	Document Number: HSMC	Rev: D
Date: Thursday, December 12, 2013	Sheet: 13	of 32

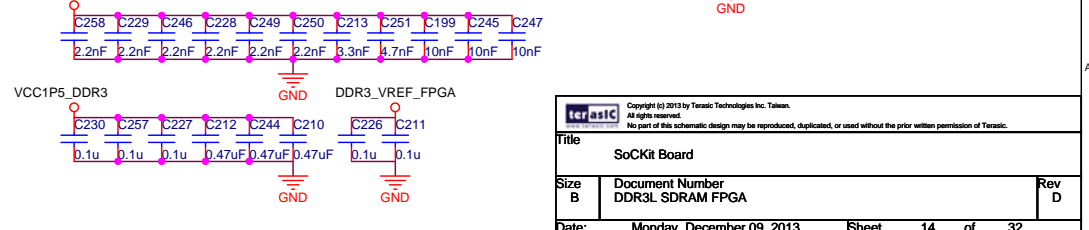
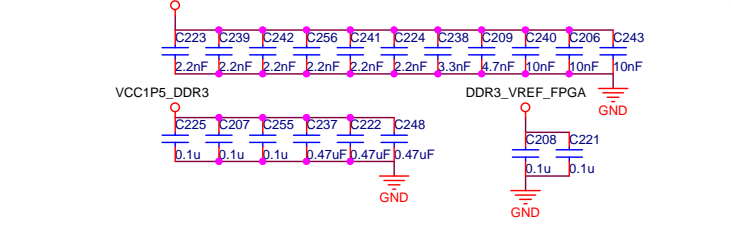




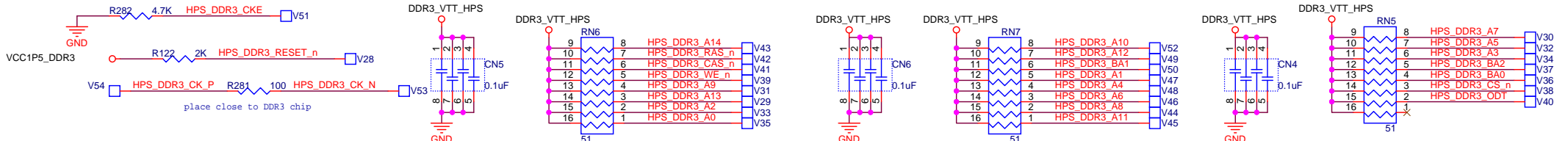
Note: you can swap the signals on the OCT resistor array (include NC pin)



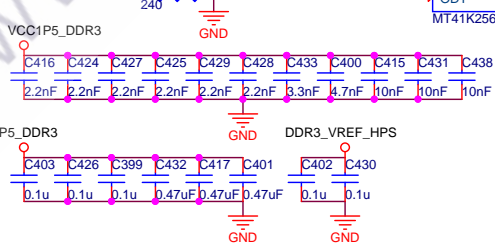
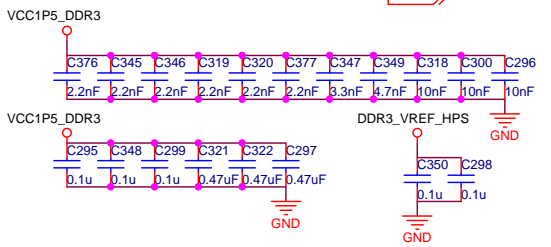
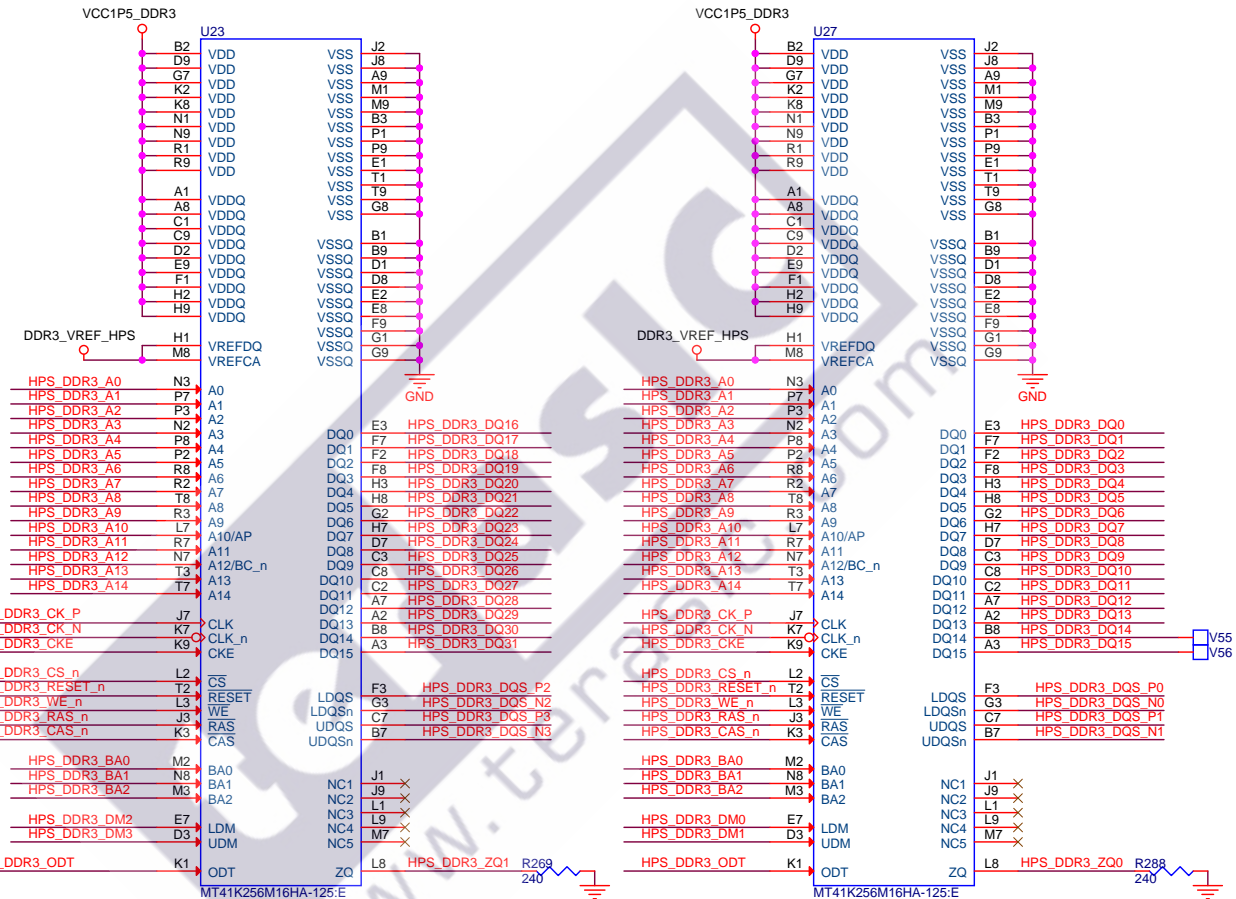
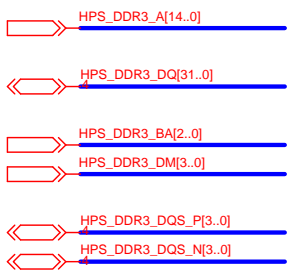
Note: you can only swap the DQ signals within x8 group (e.g. 0-7, 8-15, 16-23, 24-31, 32-39) on the DDR3 chips



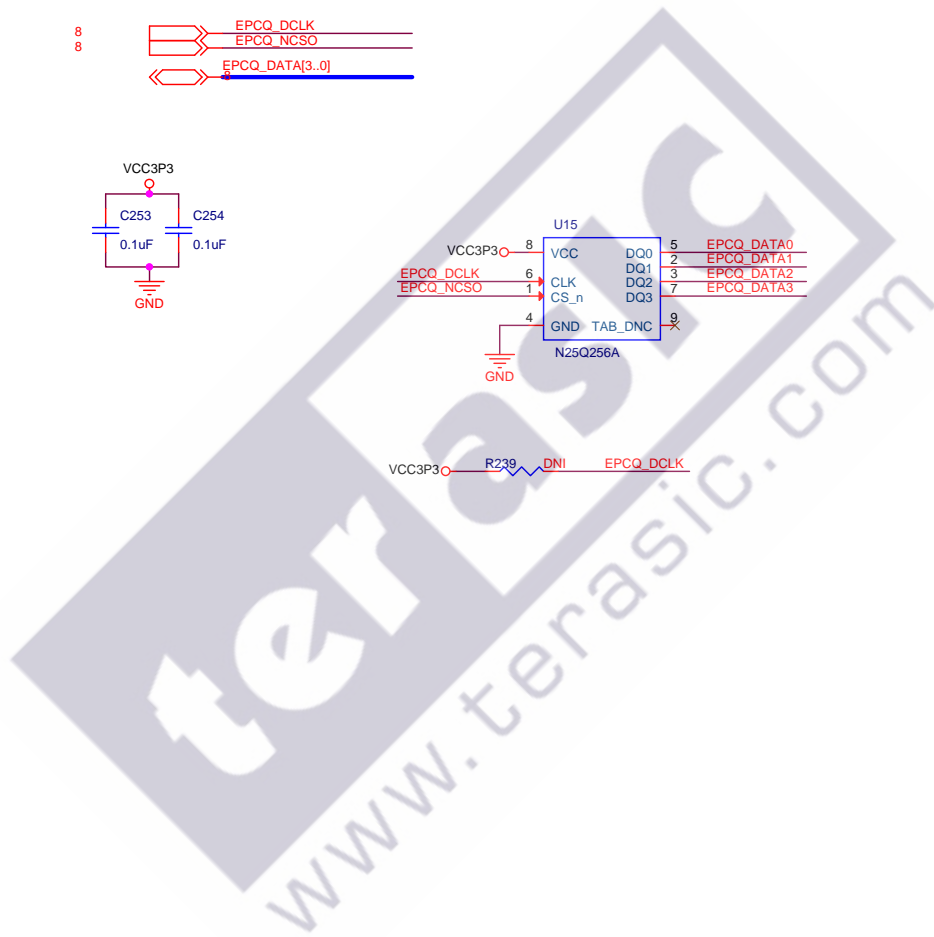
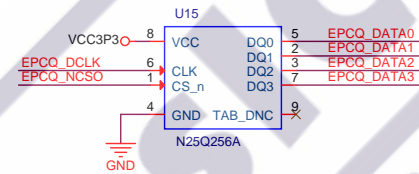
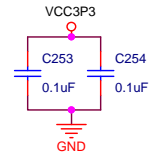
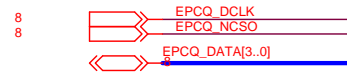
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title	
SoCKit Board	
Size	Document Number
B	DDR3L SDRAM FPGA
Date:	Monday, December 09, 2013
Sheet	14 of 32
Rev	D




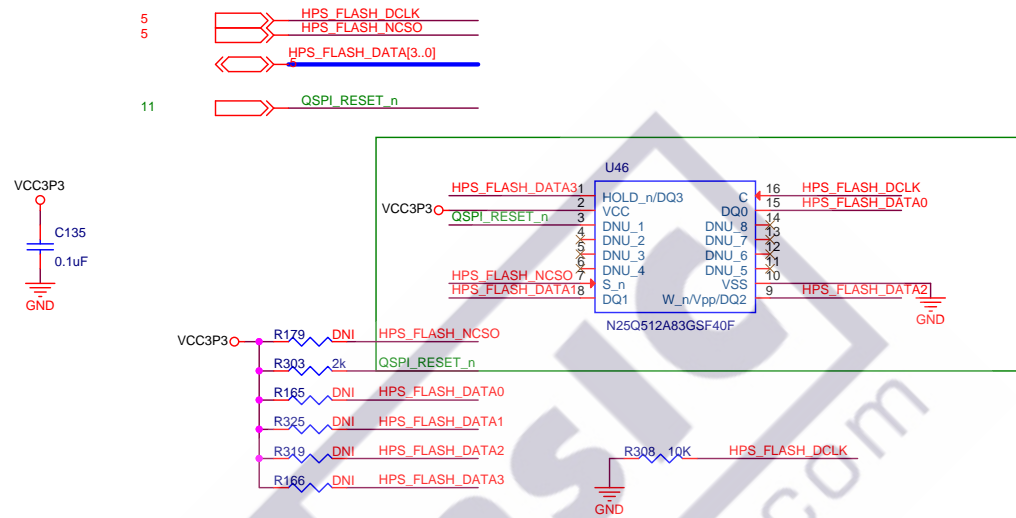
Note: you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31) on the DDR3 chips Note: you can swap the signals on the OCT resistor array(include NC pin)



Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.			
Title			
SoCKit Board			
Size	Document Number		Rev
B	DDR3L SDRAM HPS		D
Date:	Monday, December 09, 2013	Sheet	15 of 32




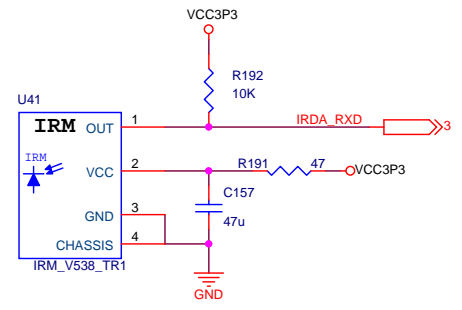
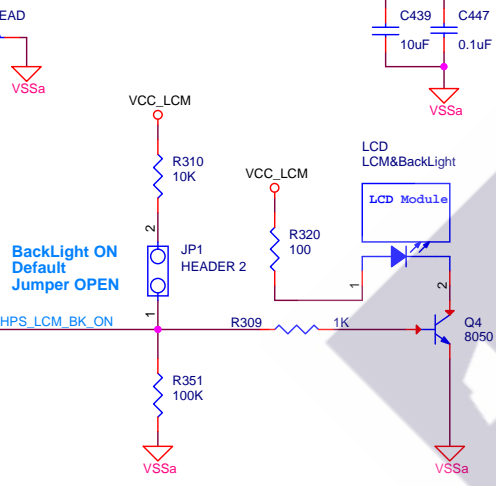
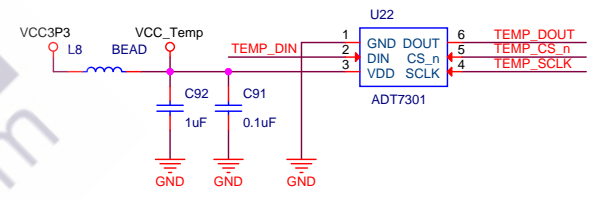
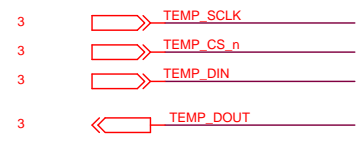
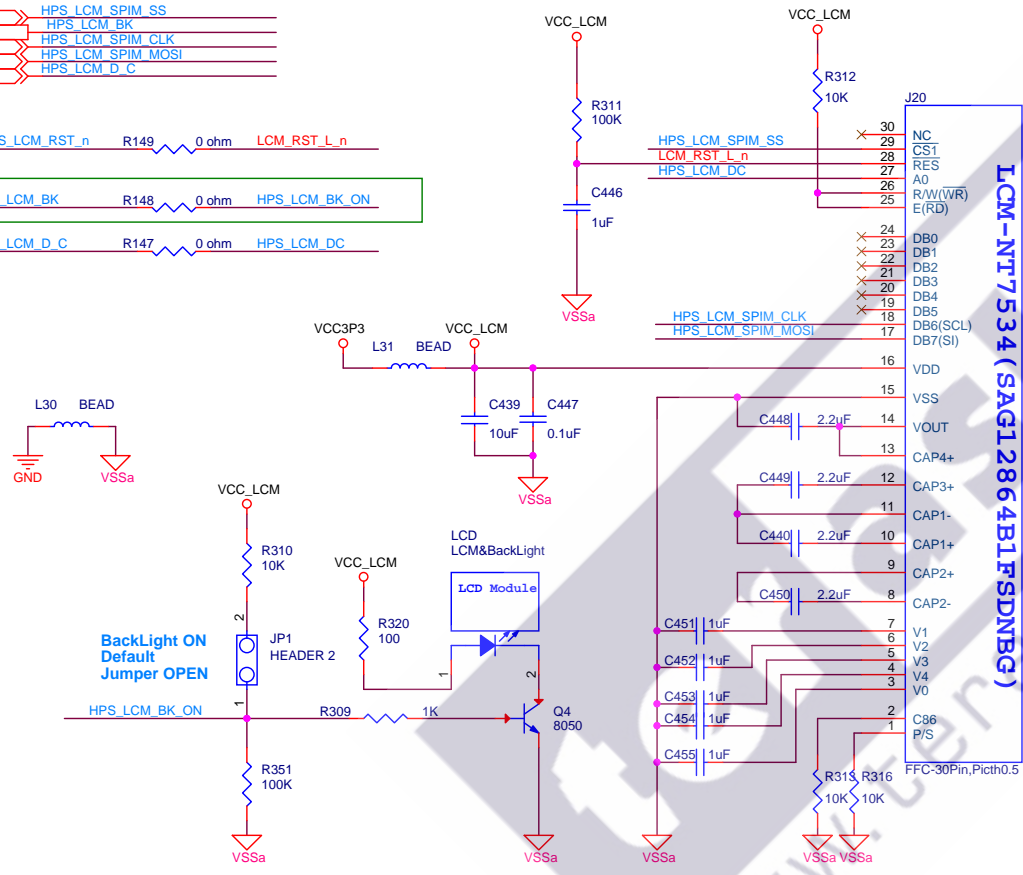
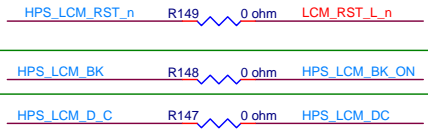
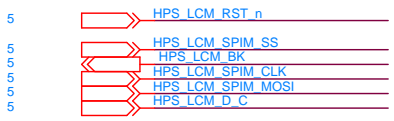
 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
SoCKit Board		
Size	Document Number	Rev
B	EPCQ	D
Date:	Monday, December 09, 2013	Sheet 16 of 32



Note: place a pull down resistor on the FLASH\_DCLK wire at the Master



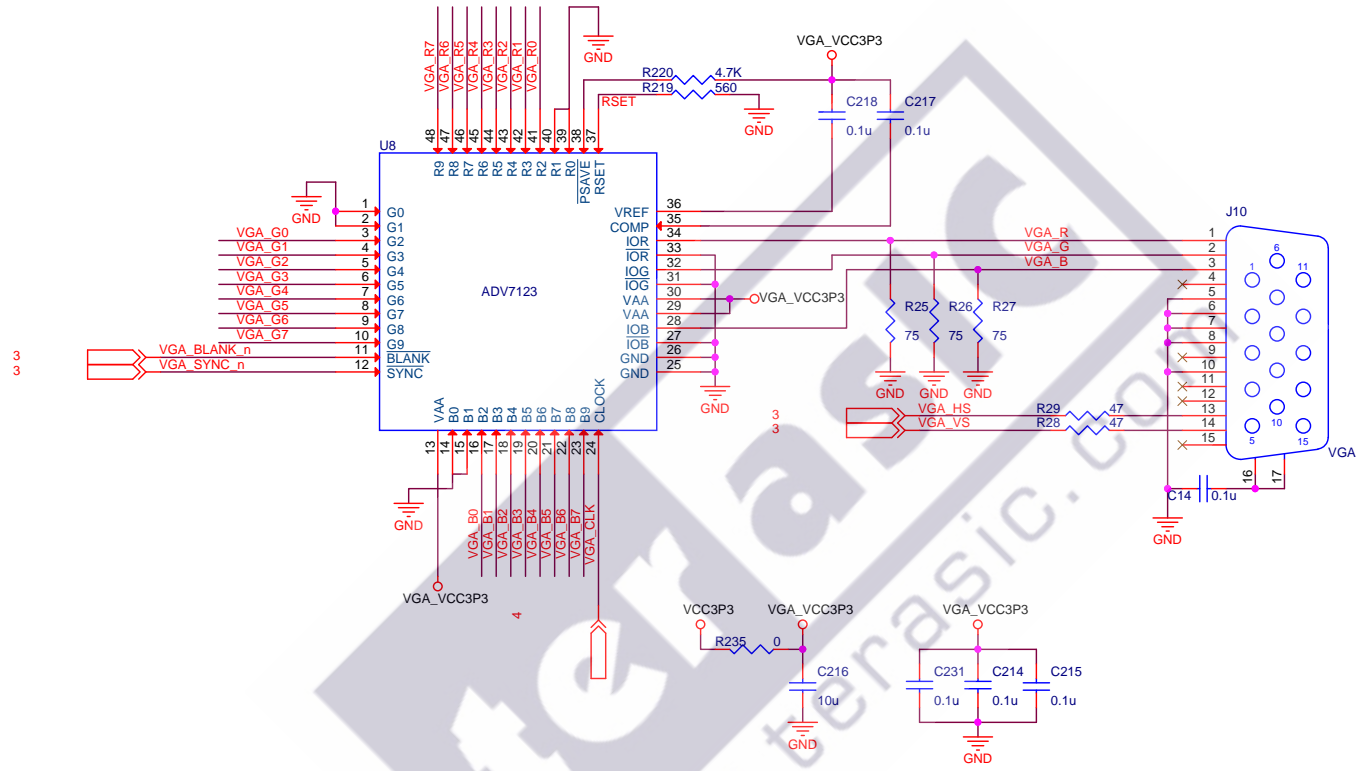
 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
SoCKit Board		
Size	Document Number	Rev
B	QSPI FLASH HPS	D
Date:	Wednesday, March 12, 2014	Sheet 17 of 32



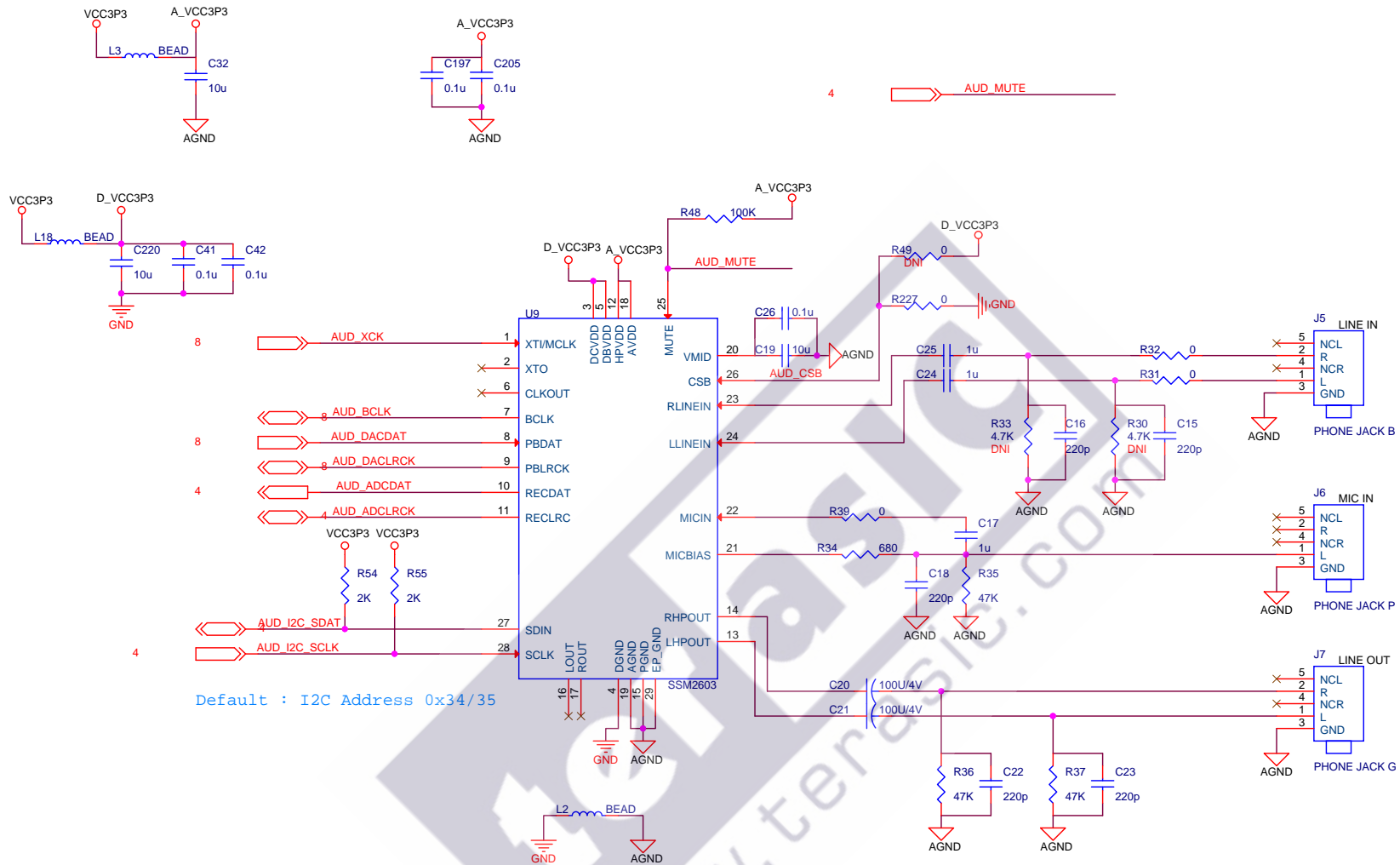
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.  
 All rights reserved.  
 No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title		
SoCKit Board		
Size	Document Number	Rev
B	LCD & Temp sensor & IRM	D
Date:	Monday, December 09, 2013	Sheet 18 of 32




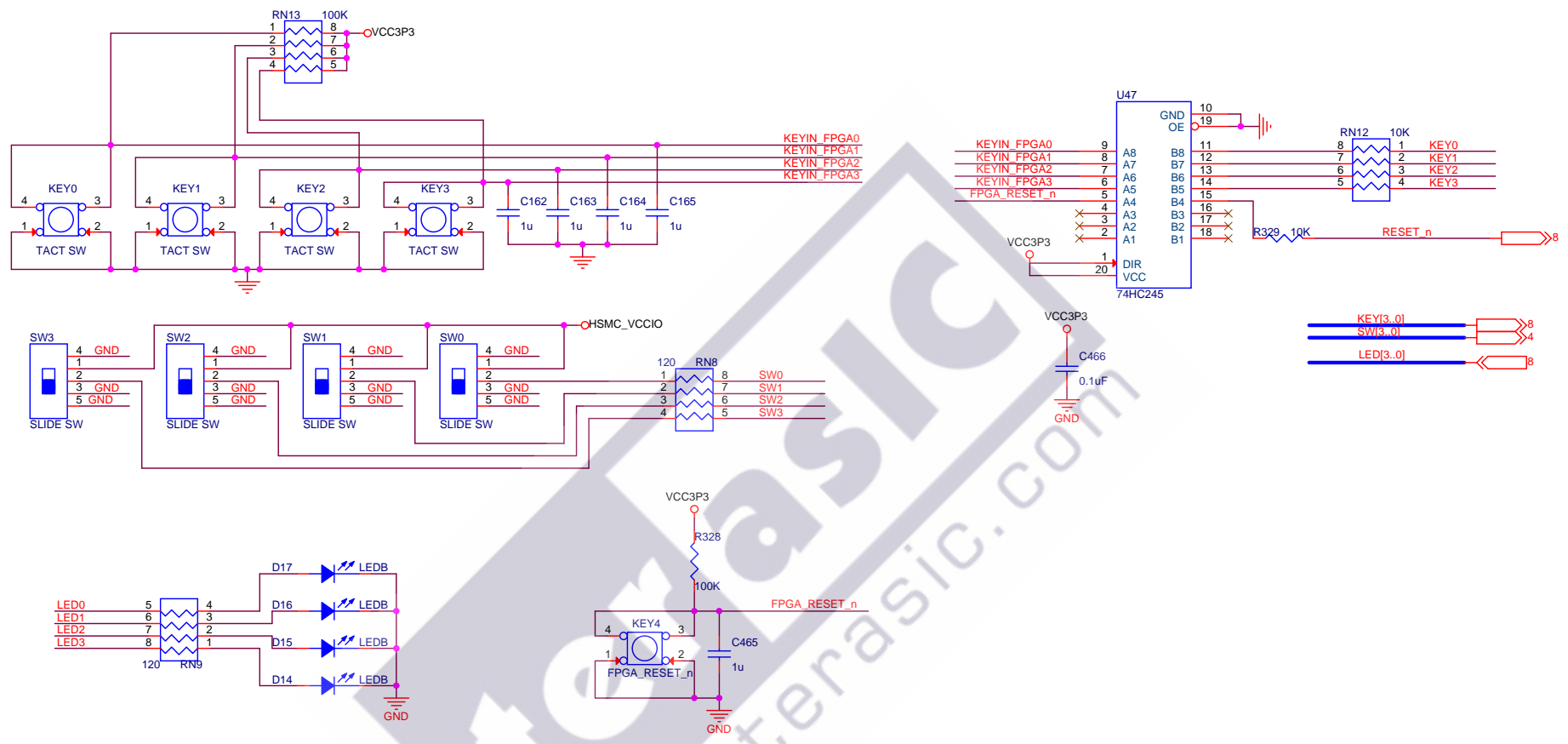


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
SoCKit Board		
Size	Document Number	Rev
B	VGA ADV7123	D
Date:	Monday, December 09, 2013	Sheet 19 of 32



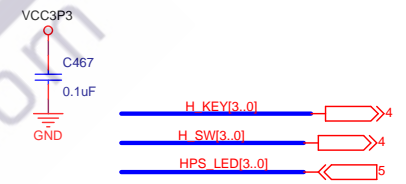
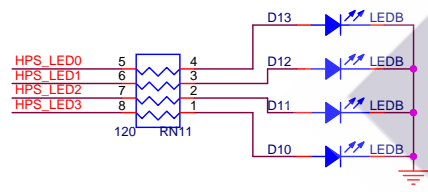
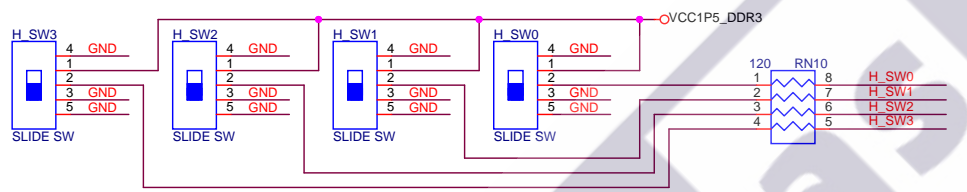
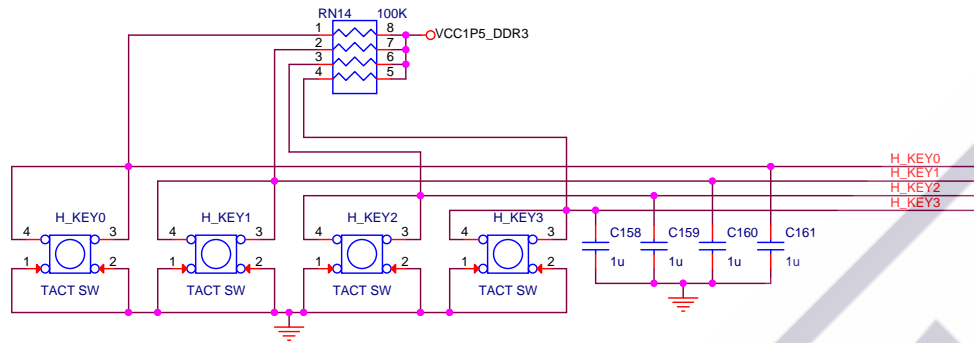
Default : I2C Address 0x34/35

 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
SoCKit Board		
Size	Document Number	Rev
B	Audio DAC	D
Date:	Monday, December 09, 2013	Sheet 20 of 32

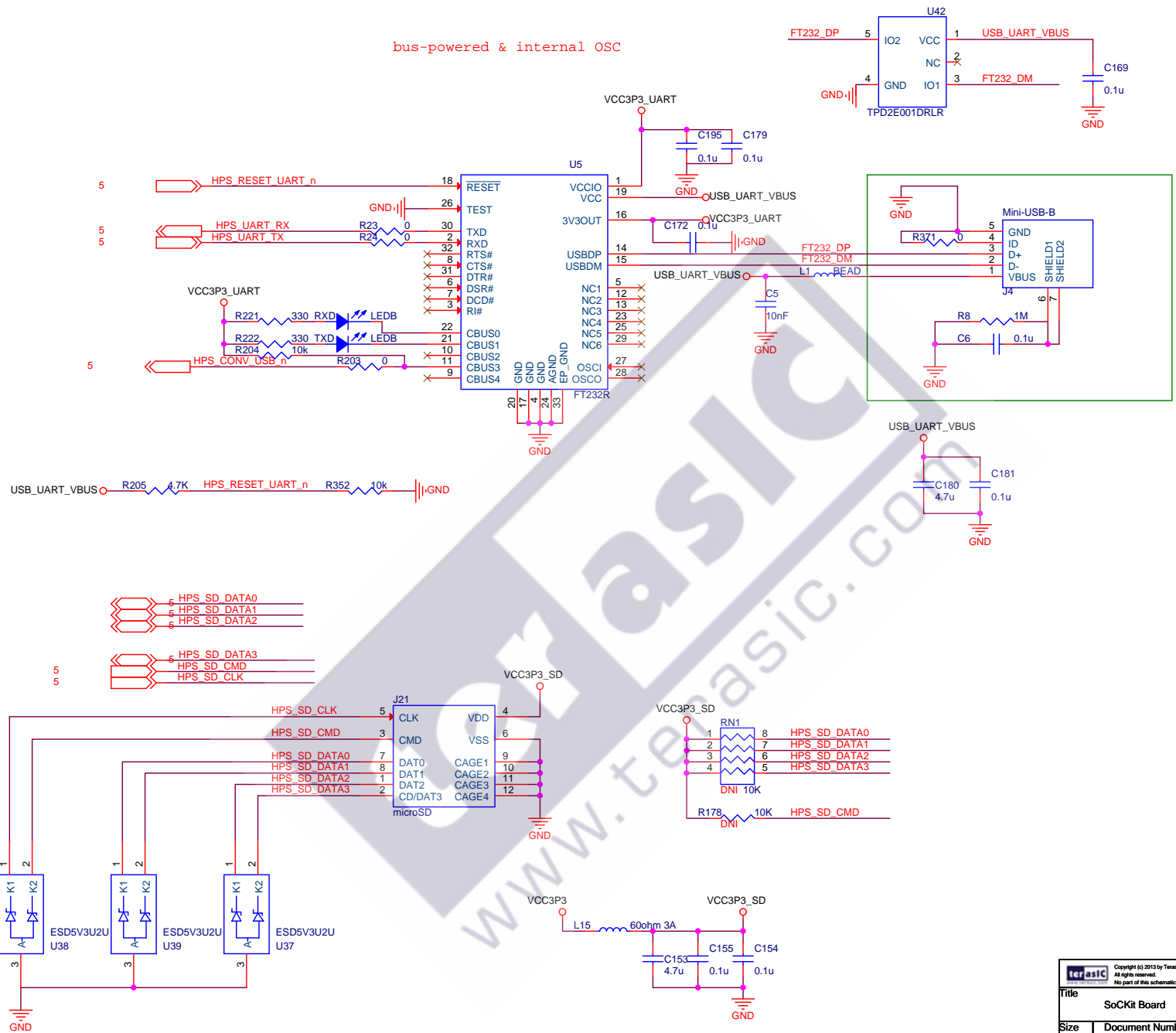


www.terasic.com

Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title	
SoCKit Board	
Size	Document Number
B	FPGA BUTTON & SW
Date:	Monday, December 09, 2013
Sheet	21 of 32
Rev	D

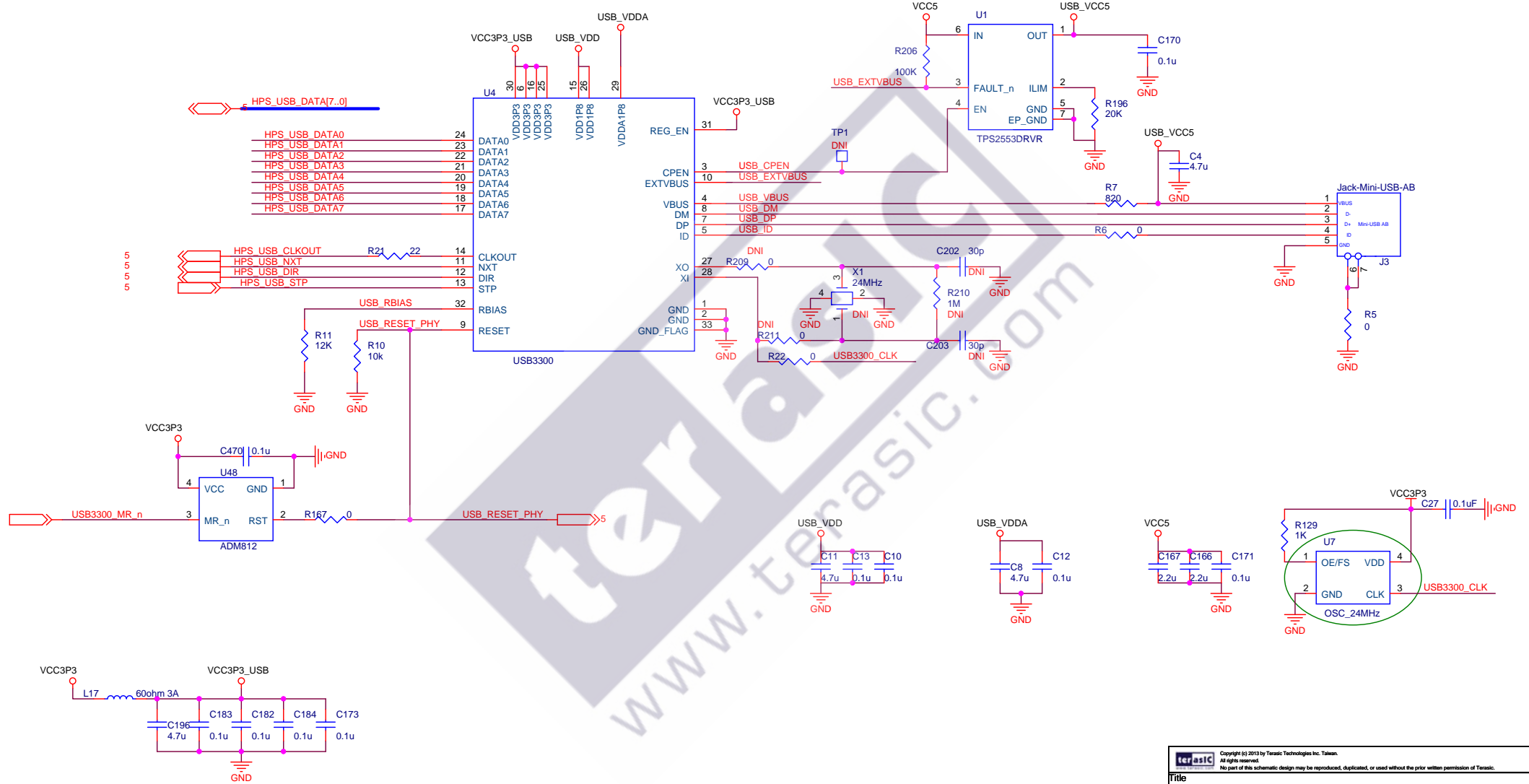


Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title	
SoCKit Board	
Size	Document Number
B	HPS BUTTON & SW
Date:	Monday, December 09, 2013
Sheet	22 of 32
Rev	D



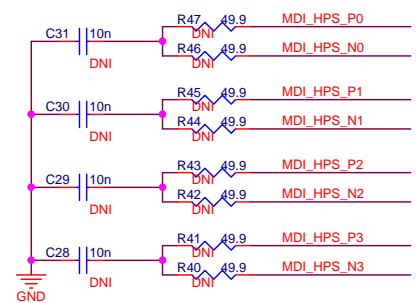
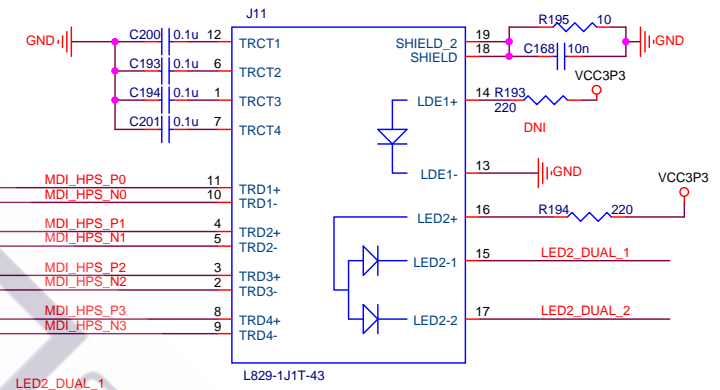
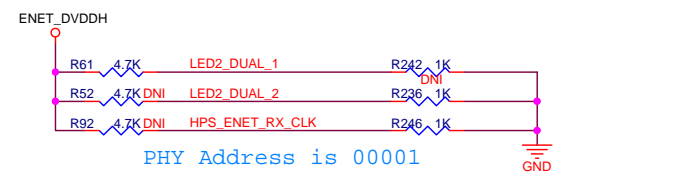
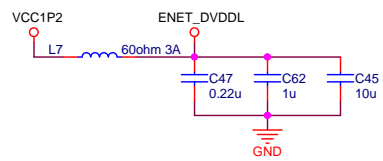
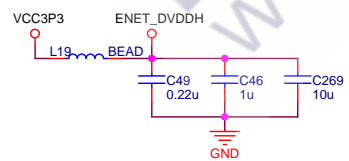
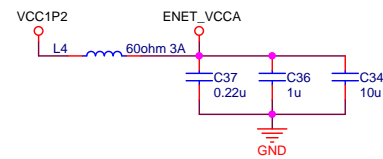
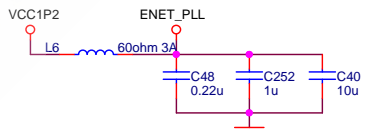
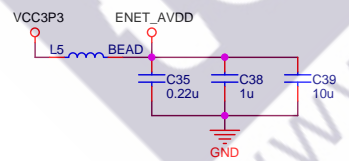
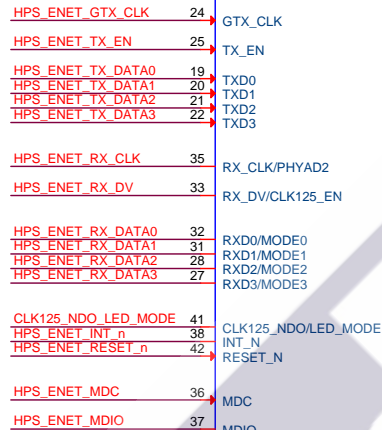
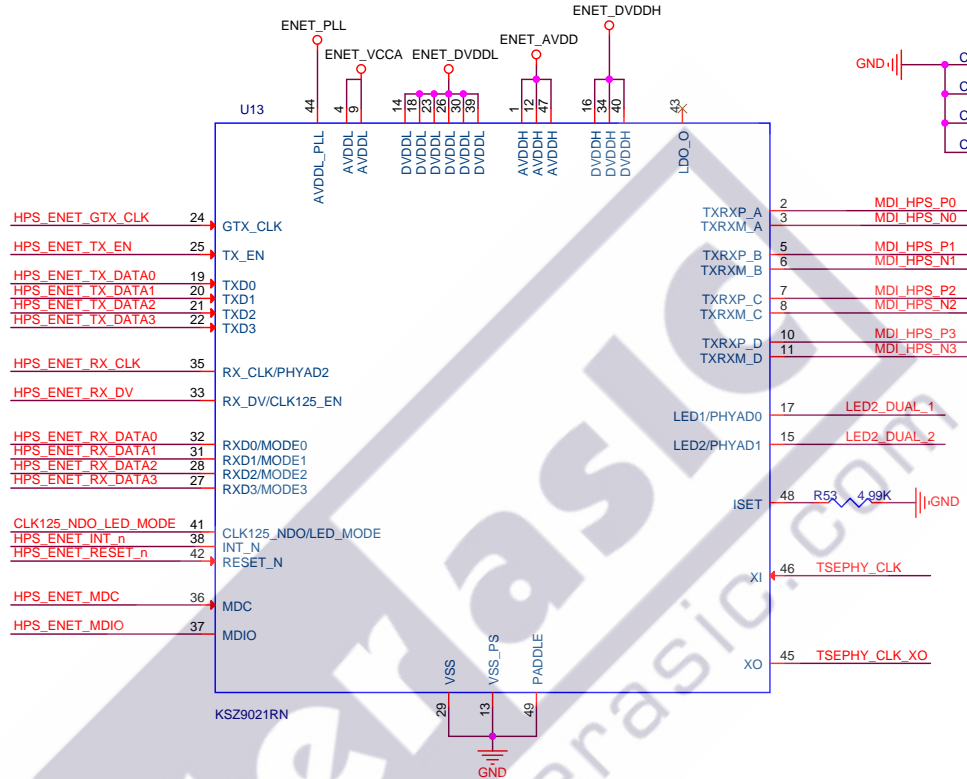
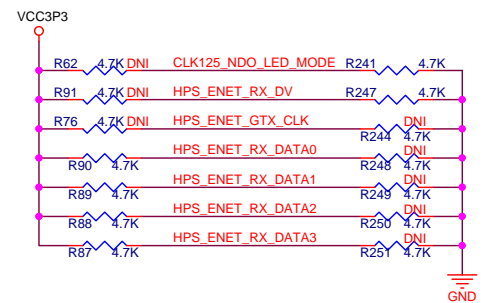
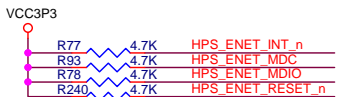
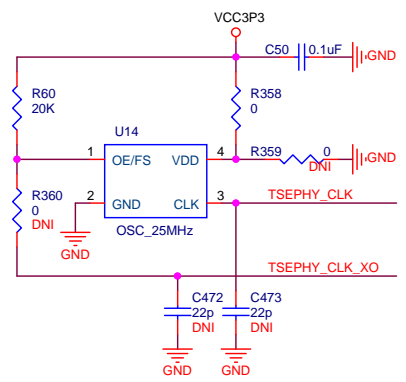
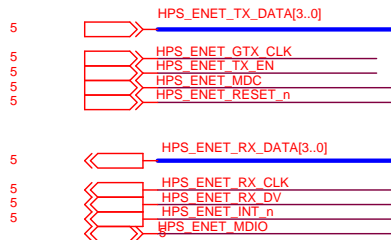
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title	
SoCKit Board	
Size	Document Number
B	USB to UART & SD CARD
Date:	Monday, December 09, 2013
Sheet	23 of 32
Rev	D





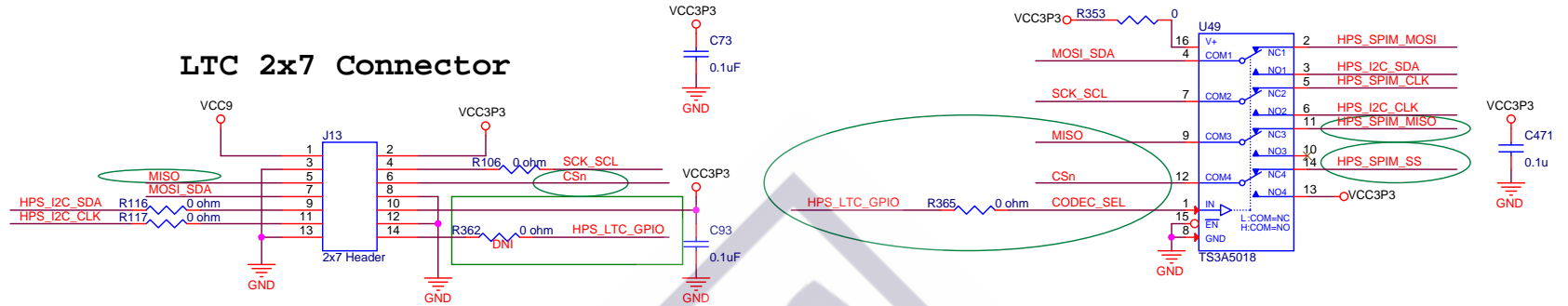
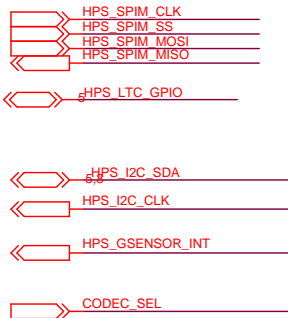
terasic  
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.  
All rights reserved.  
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title		
SoCKit Board		
Size	Document Number	Rev
B	USB3300	D
Date:	Monday, December 09, 2013	Sheet 24 of 32

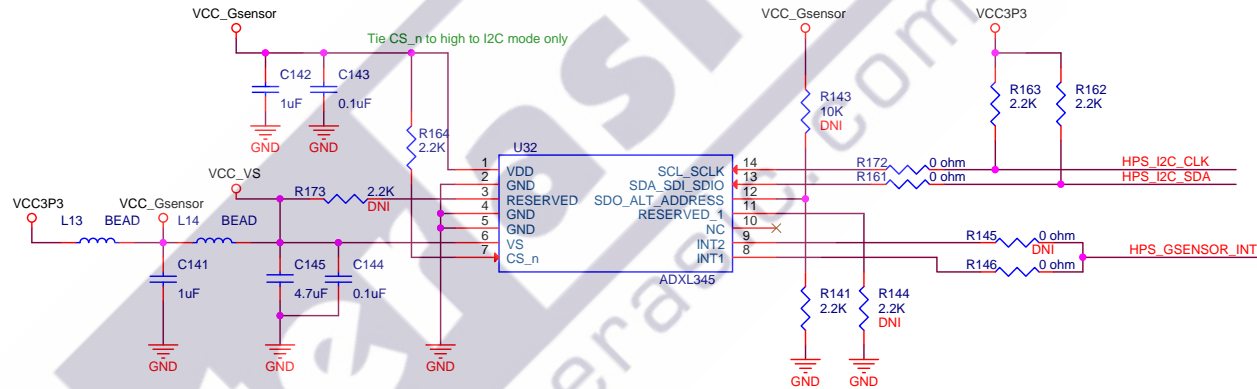


terasic  
 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan.  
 All rights reserved.  
 No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title		
SoCKit Board		
Size	Document Number	Rev
B	TSE PHY	D
Date:	Monday, December 09, 2013	Sheet 25 of 32

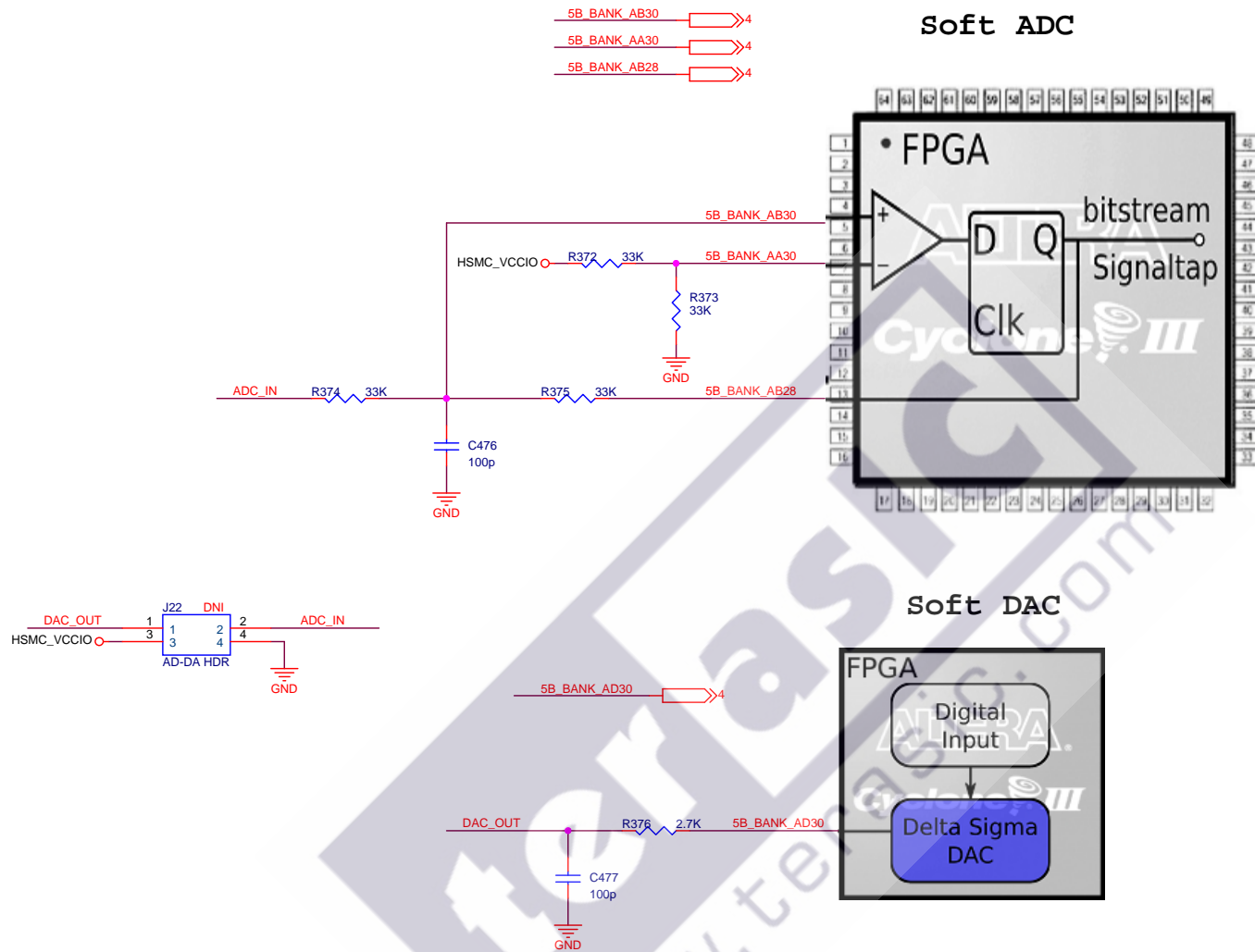



### Digital Accelerometer

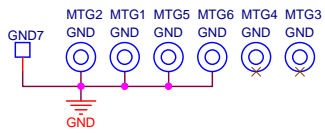


Default: I2C Address 0xA6/0xA7

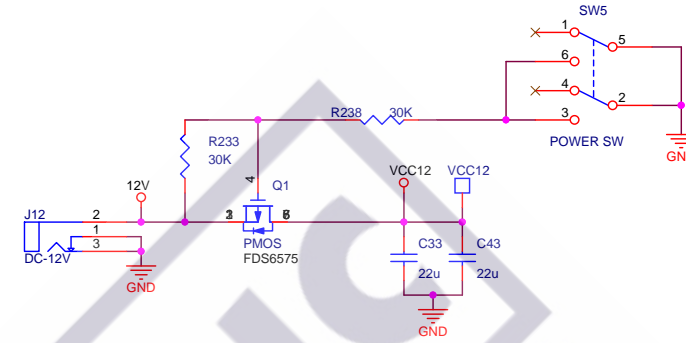
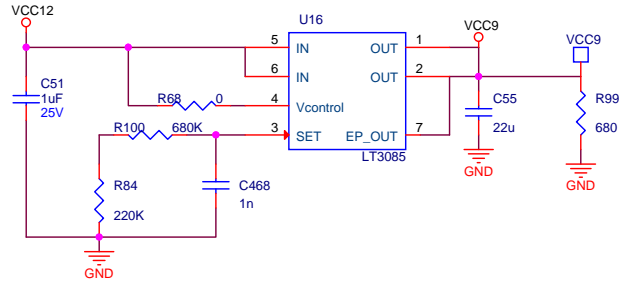
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
SoCKit Board		
Size	Document Number	Rev
B	LTC Connector & G sensor	D
Date:	Monday, December 09, 2013	Sheet 26 of 32



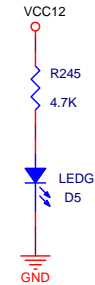
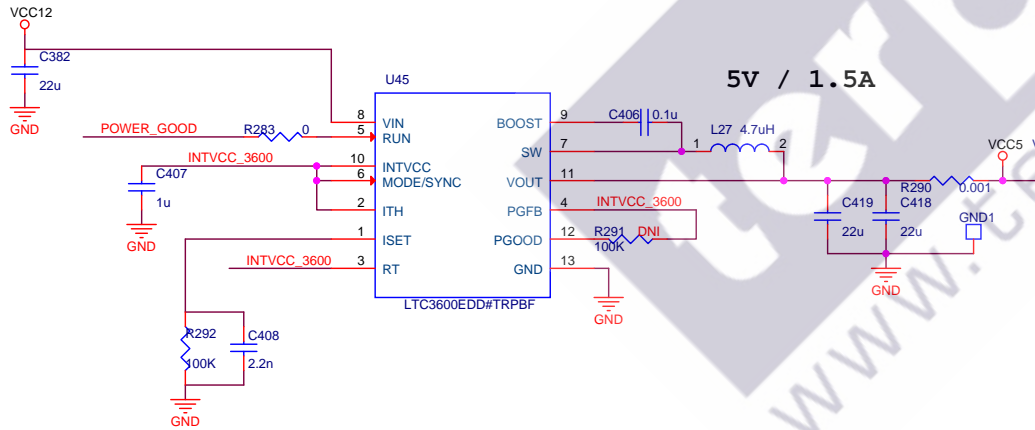
 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
SoCKit Board		
Size	Document Number	Rev
B	Soft ADC & DAC	D
Date:	Wednesday, December 11, 2013	Sheet 27 of 32



9V / 50mA

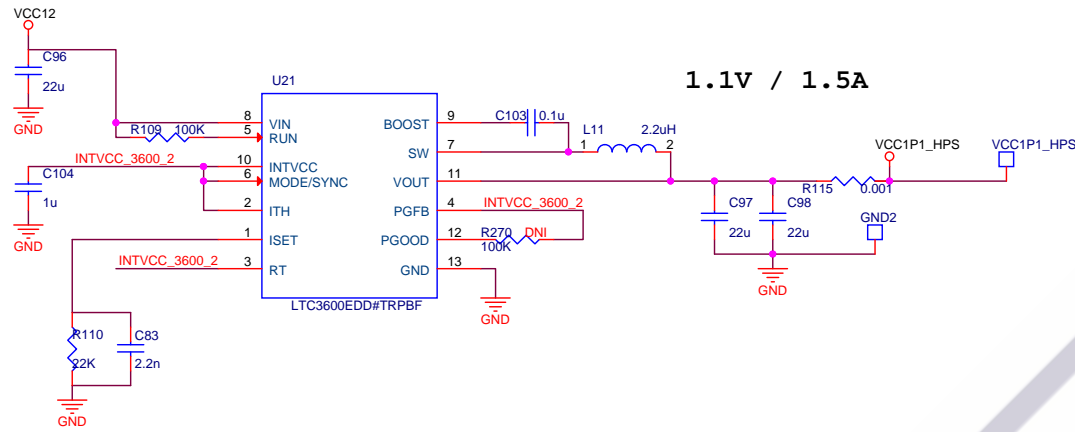


5V / 1.5A

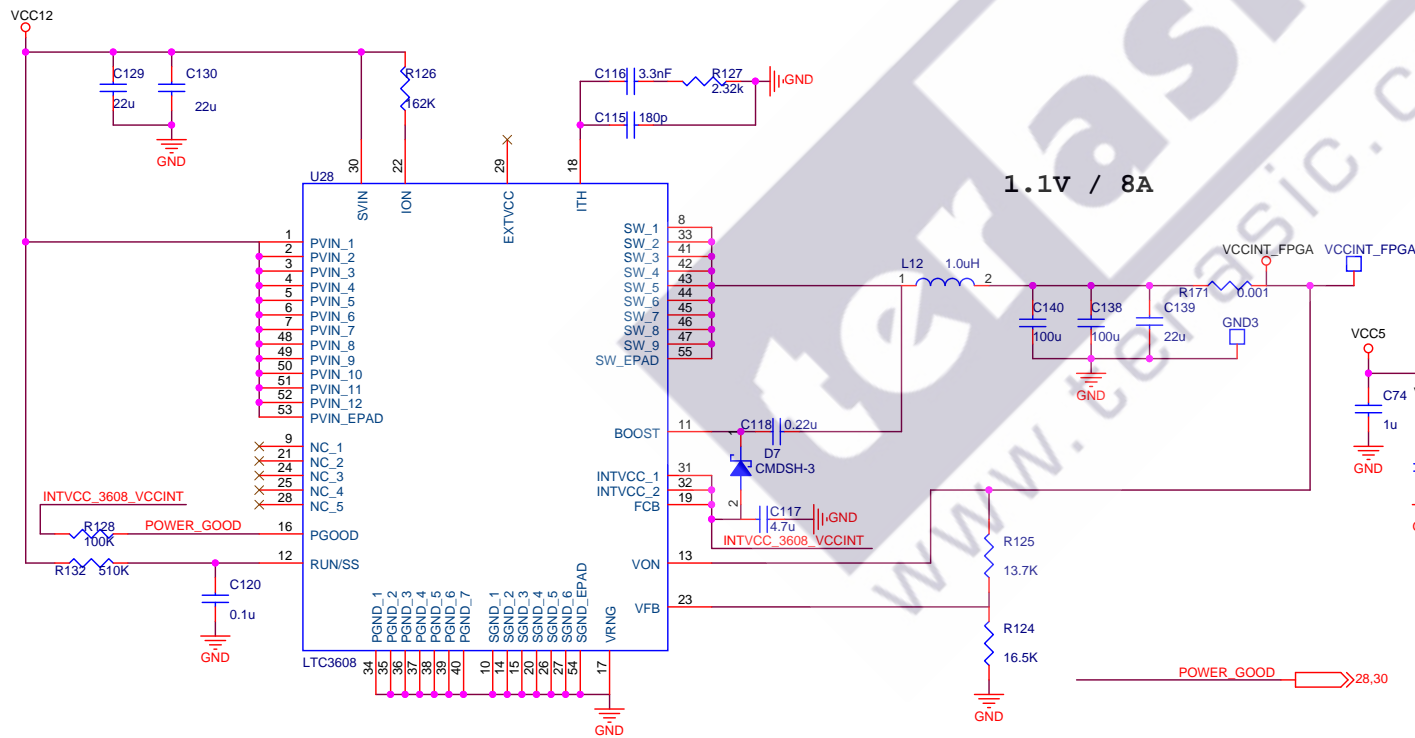
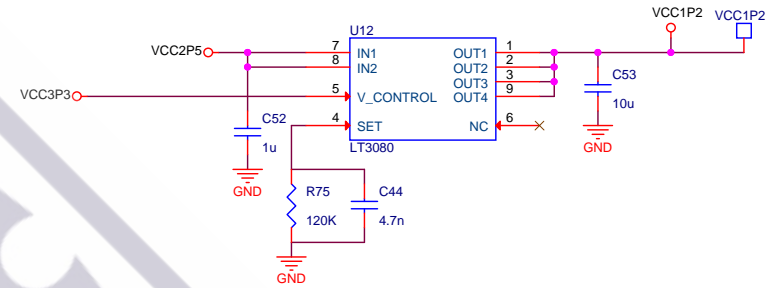


29,30 POWER\_GOOD

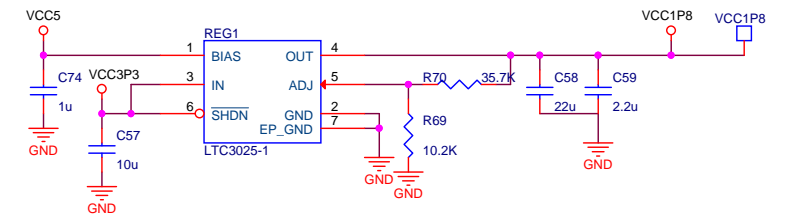
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title	
SoCKit Board	
Size	Document Number
B	Power - 9V & 5V
Date:	Monday, December 09, 2013
Sheet	28 of 32
Rev	D



**1.2V / 563mA (up to 1.1A)**

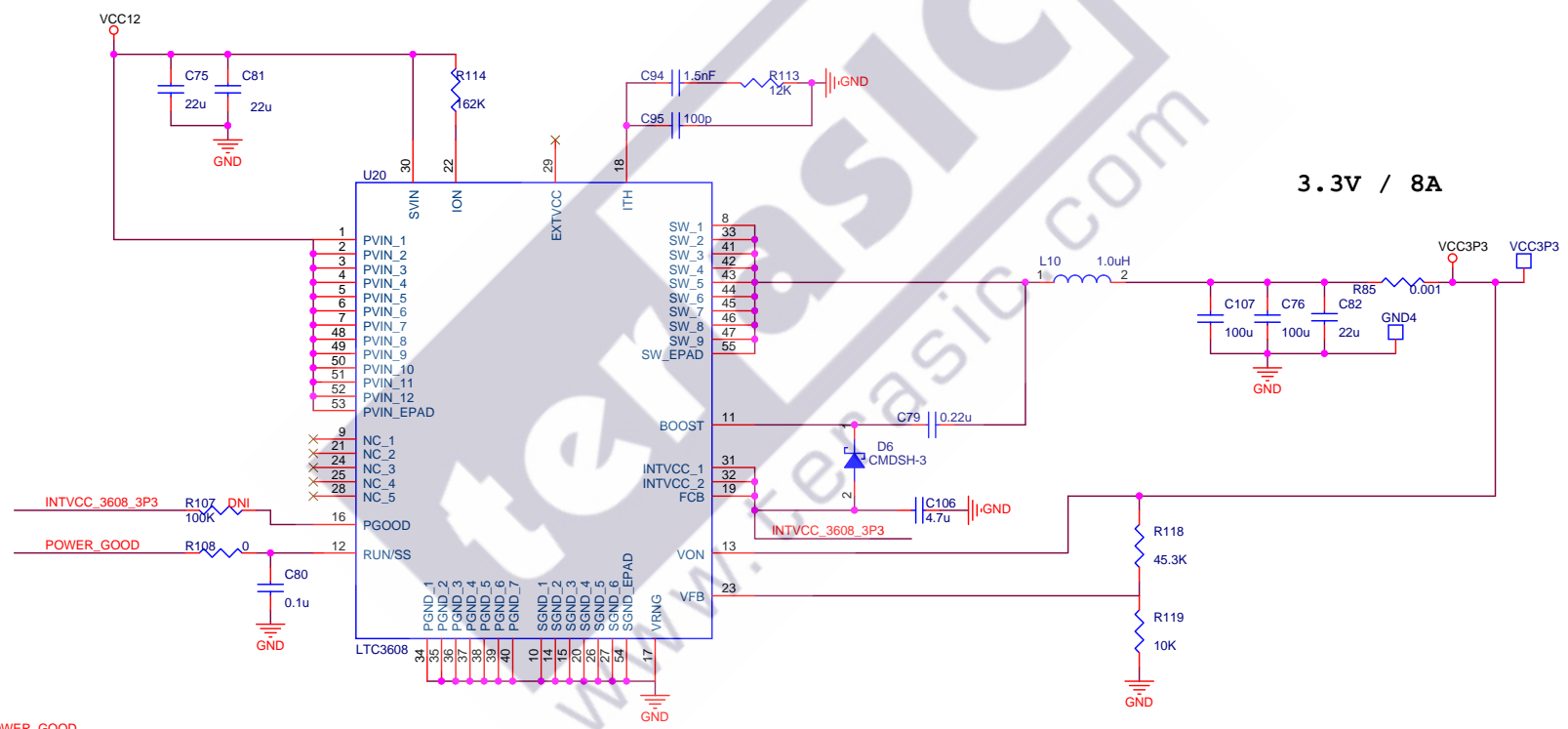
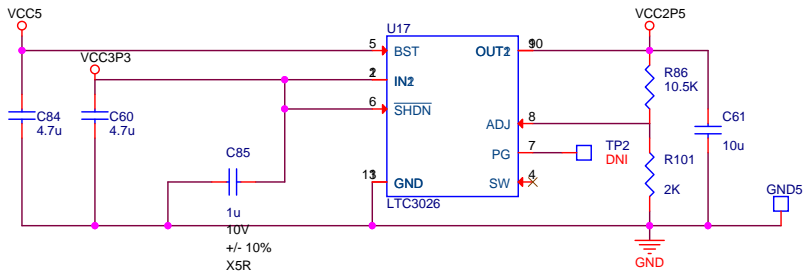


**1.8V / 0.5A**



Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title	
SoCKit Board	
Size B	Document Number
	Power - 1.1V & 1.2V
Date:	Monday, December 09, 2013
Sheet	29 of 32

2.5V / 1.5A



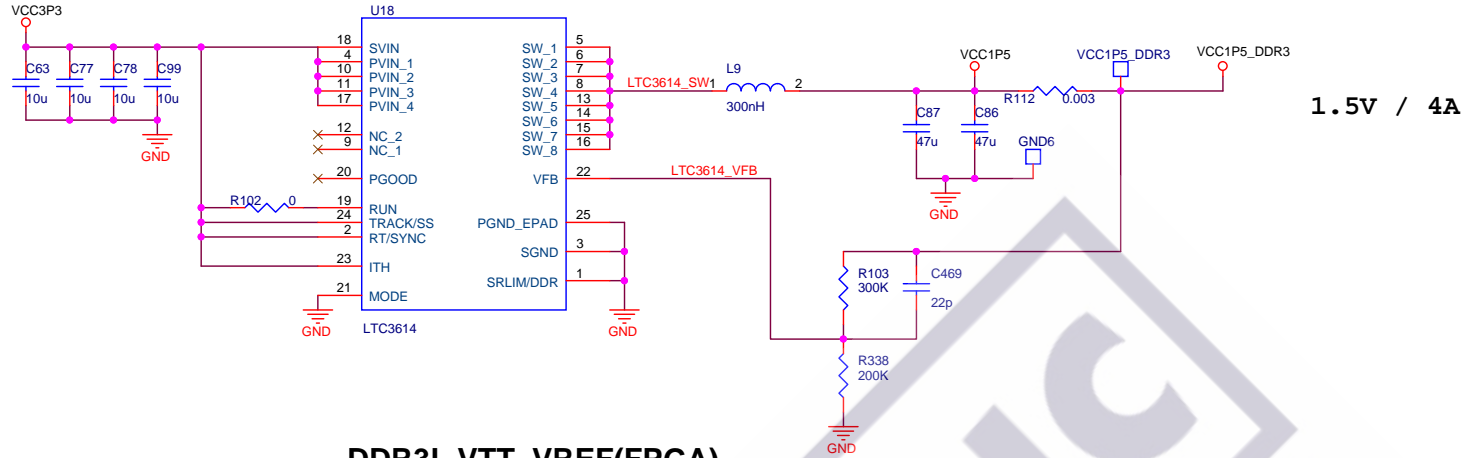
3.3V / 8A

28,29 POWER\_GOOD

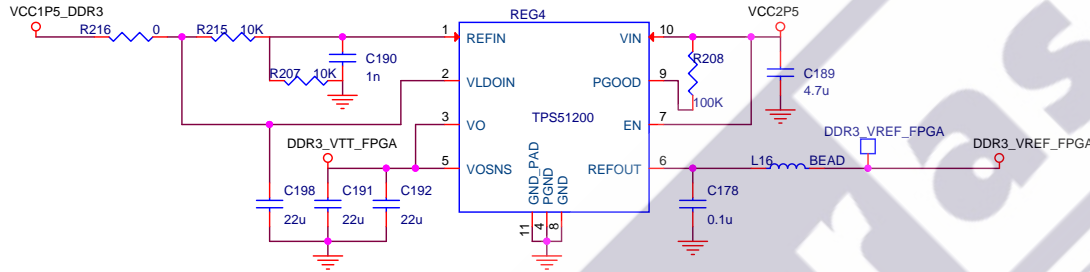
Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
SoCKit Board		
Size B	Document Number	Rev D
Power - 3.3V & 2.5V		
Date:	Monday, December 09, 2013	Sheet 30 of 32



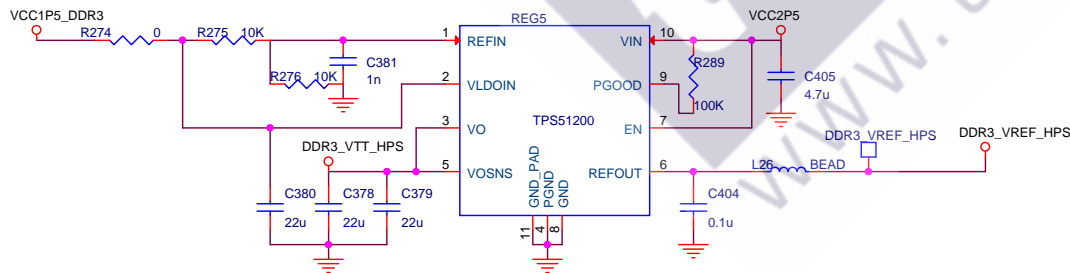
### DDR3L VDD,VDDQ




### DDR3L VTT, VREF(FPGA)

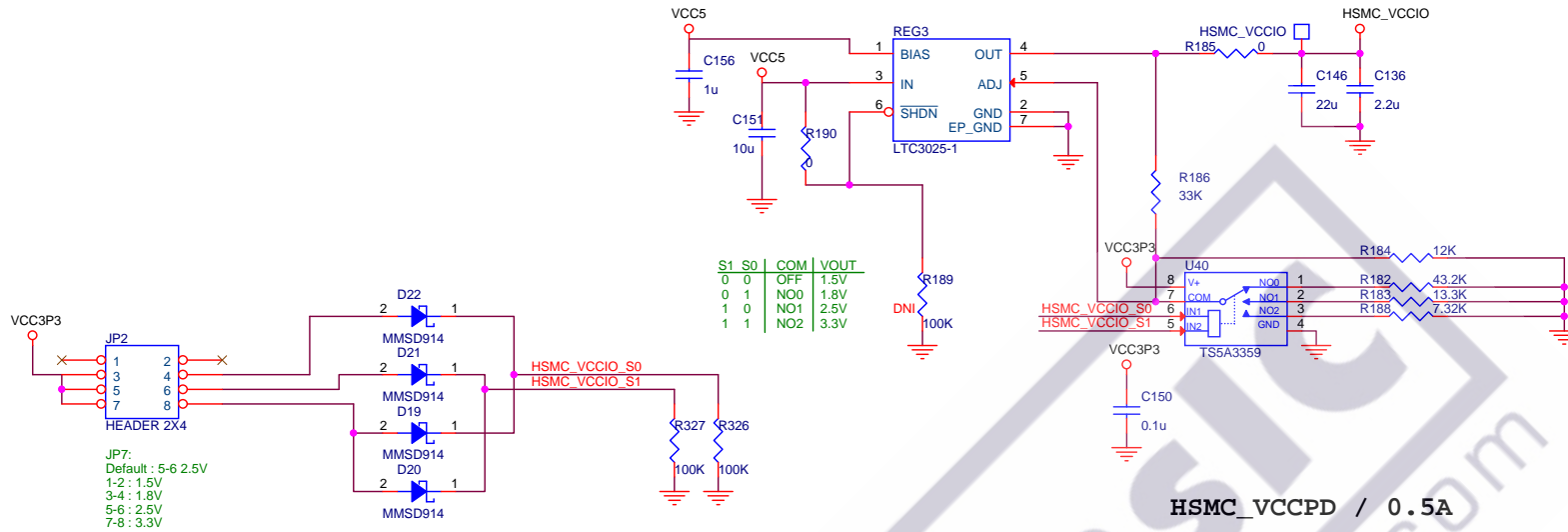


### DDR3L VTT, VREF(HPS)



 Copyright (c) 2013 by Terasic Technologies Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
SoCKit Board		
Size	Document Number	Rev
B	Power - 1.5V	D
Date:	Monday, December 09, 2013	Sheet 31 of 32

### HSMC\_VCCIO / 0.5A



### HSMC\_VCCPD / 0.5A

