


SoCKit

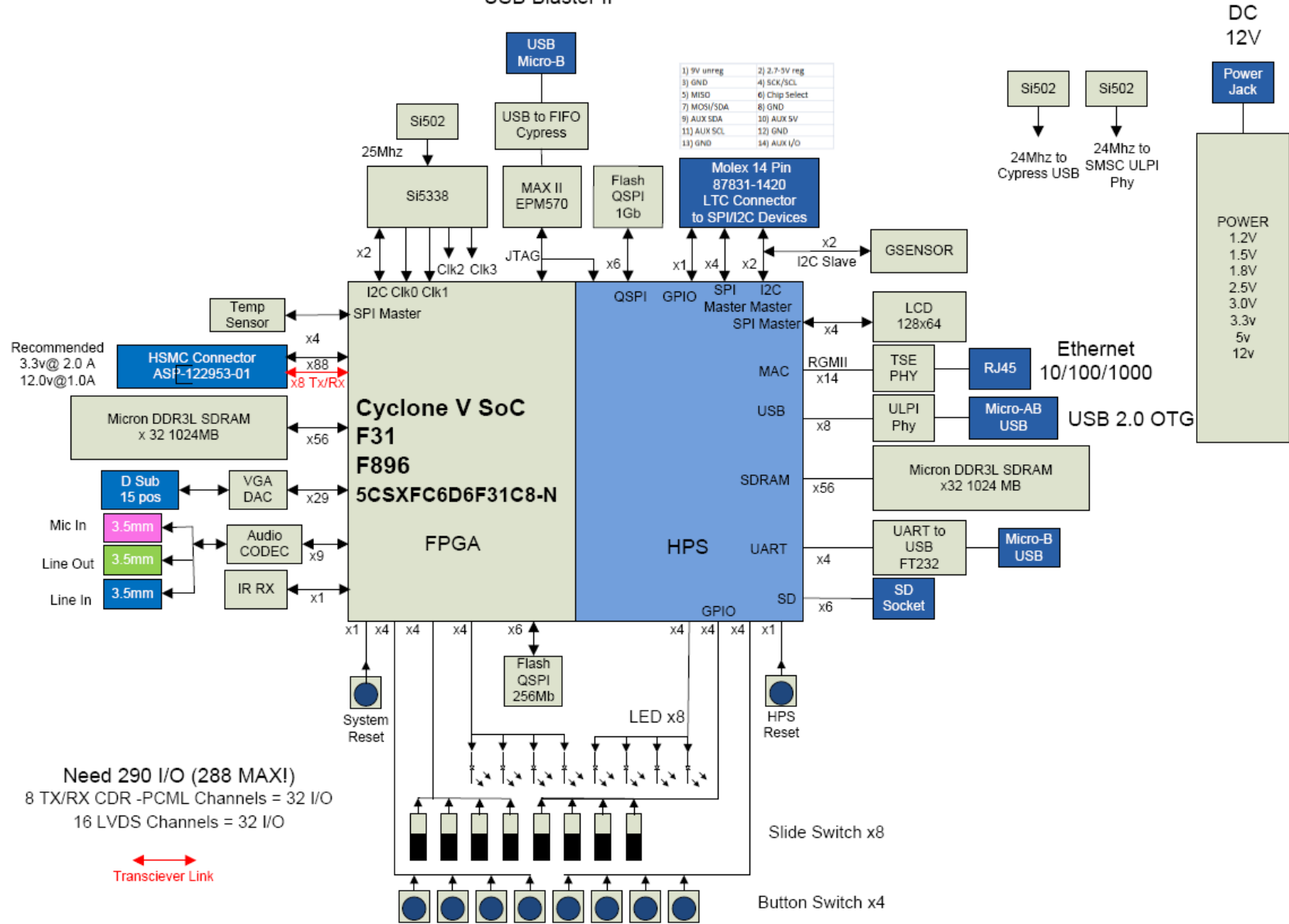
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USB Blaster II

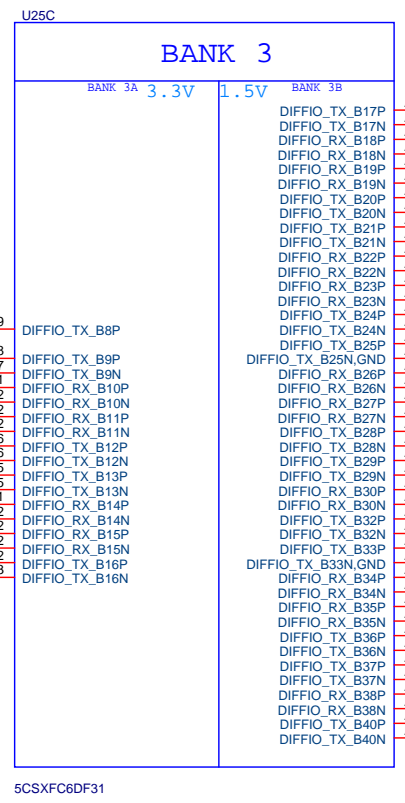


VGA_R[7..0] 19

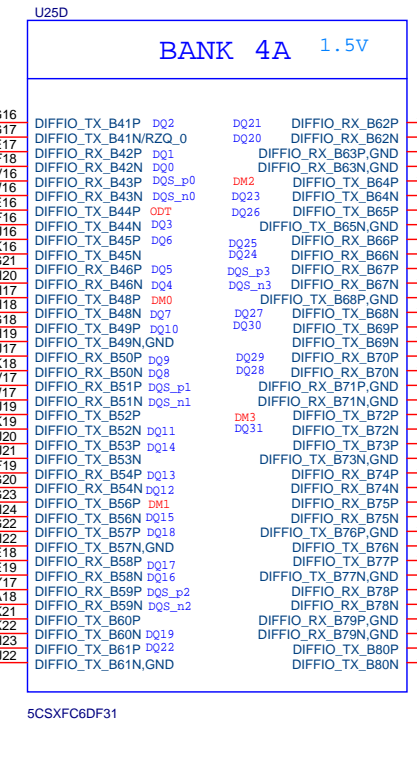
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 11 USB RESET_n
 11 USB OE_n
 11 USB RD_n
 11 USB WR_n
 11 USB SCL
 11 USB FULL
 11 USB EMPTY
 11 USB_SDA

11 USB_B2_DATA[7..0]

14 FPGA_DDR3_CK_p
 14 FPGA_DDR3_CK_n
 14 FPGA_DDR3_CKE
 14 FPGA_DDR3_RESET_n
 14 FPGA_DDR3_WE_n
 14 FPGA_DDR3_RAS_n
 14 FPGA_DDR3_CAS_n
 14 FPGA_DDR3_CS_n
 14 FPGA_DDR3_ODT
 14 FPGA_DDR3_A[14..0]
 14 FPGA_DDR3_DM[3..0]
 14 FPGA_DDR3_BA[2..0]
 14 FPGA_DDR3_DQ[31..0]
 14 FPGA_DDR3_DQS_p[3..0]
 14 FPGA_DDR3_DQS_n[3..0]



18< TEMP_SCLK AF9
 18< TEMP_CS_n AF8
 18< TEMP_DIN AG7
 18< TEMP_DOUT AG1
 18< IRDA_RXD AH2
 VGA_R1 AA12
 VGA_R2 AB12
 VGA_R3 AF6
 VGA_R4 AG6
 VGA_R0 AG5
 VGA_R6 AH5
 VGA_R7 AJ1
 VGA_R5 AJ2
 VGA_VS AC12
 VGA_HS AD12
 VGA_SYNC_n AG2
 VGA_BLANK_n AH3

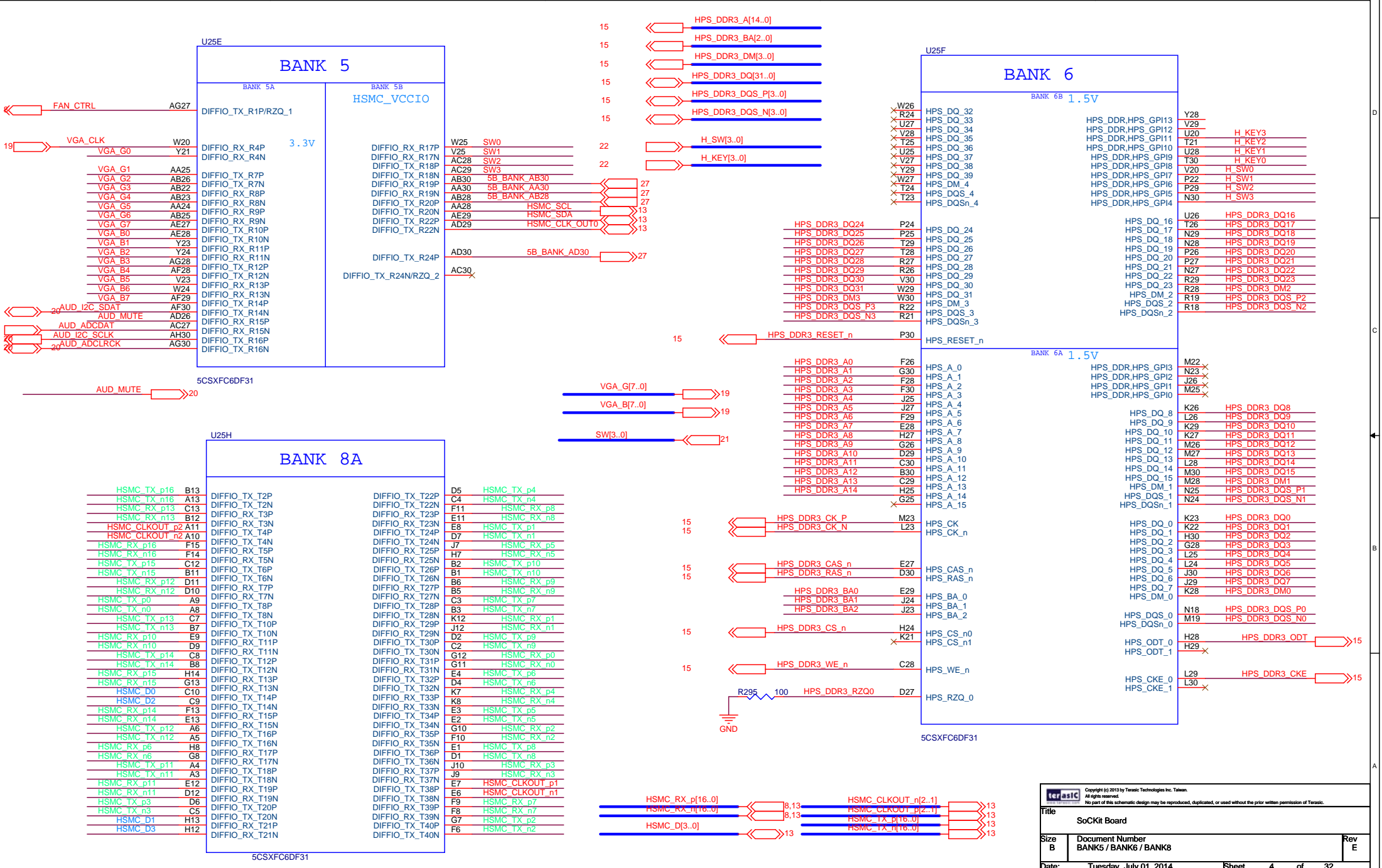


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Title: SoCKit Board

Size B Document Number: BANK3 & BANK4 Rev E

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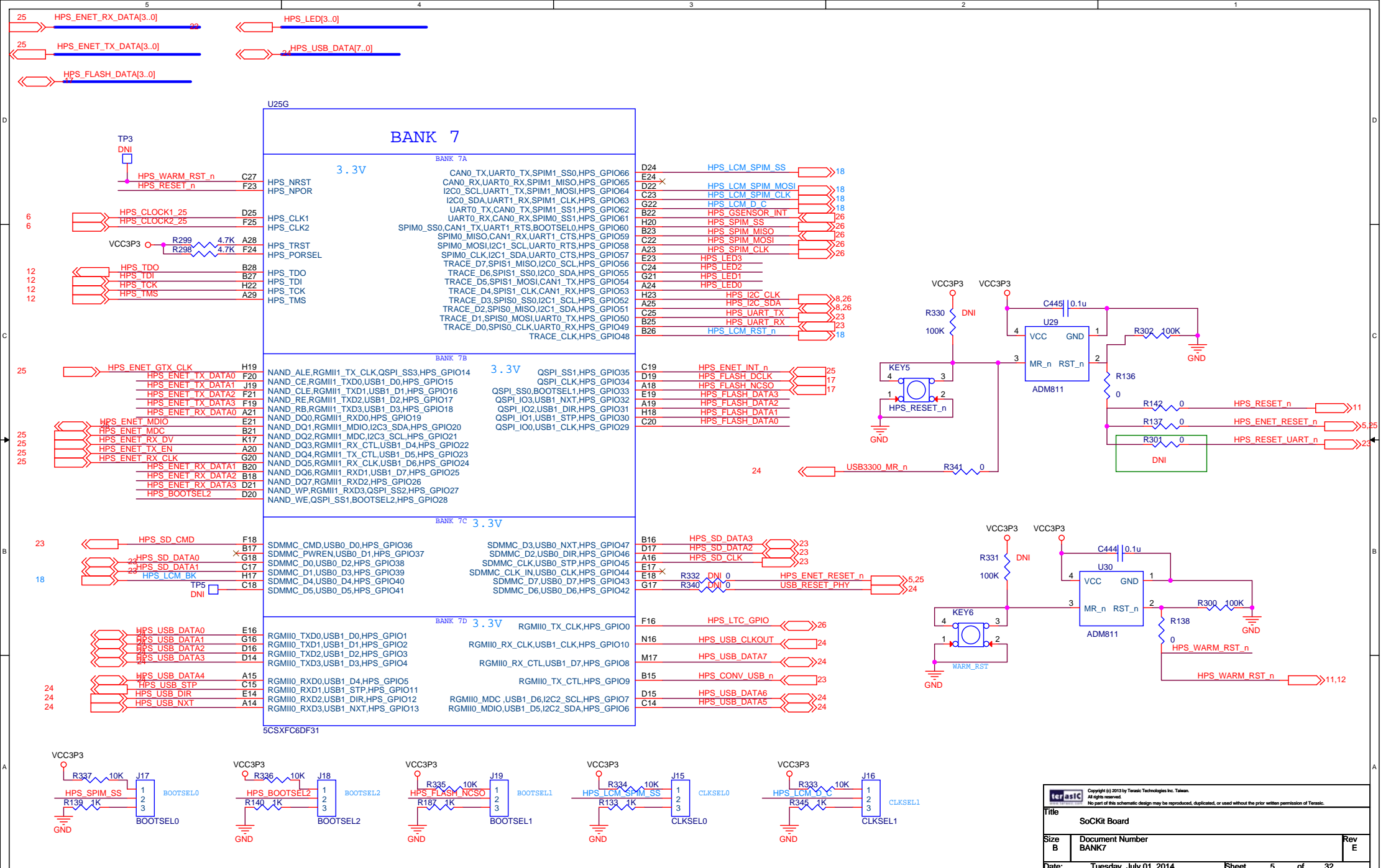
SoCKit Board

Document Number: BANK5 / BANK6 / BANK8

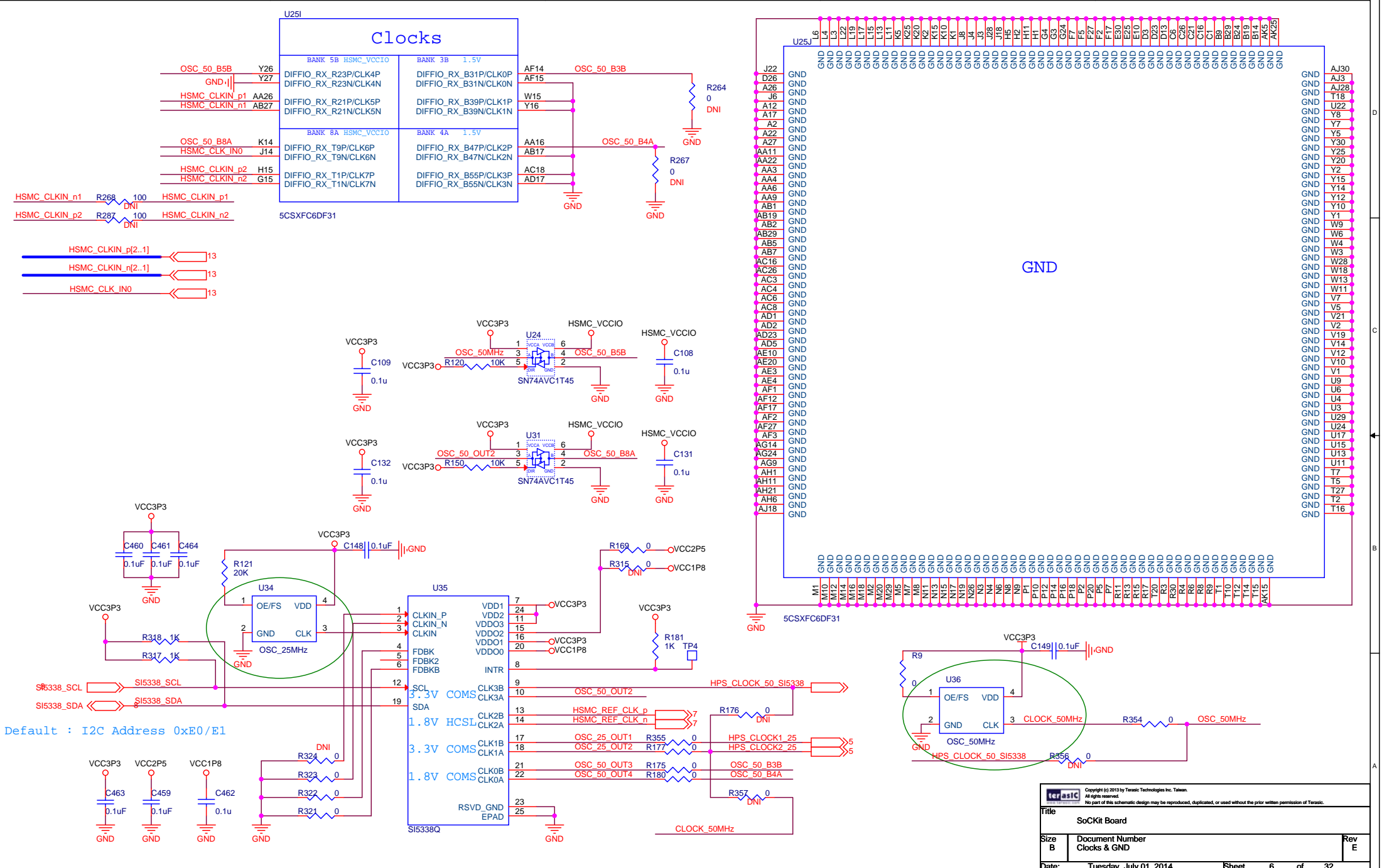
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Rev E



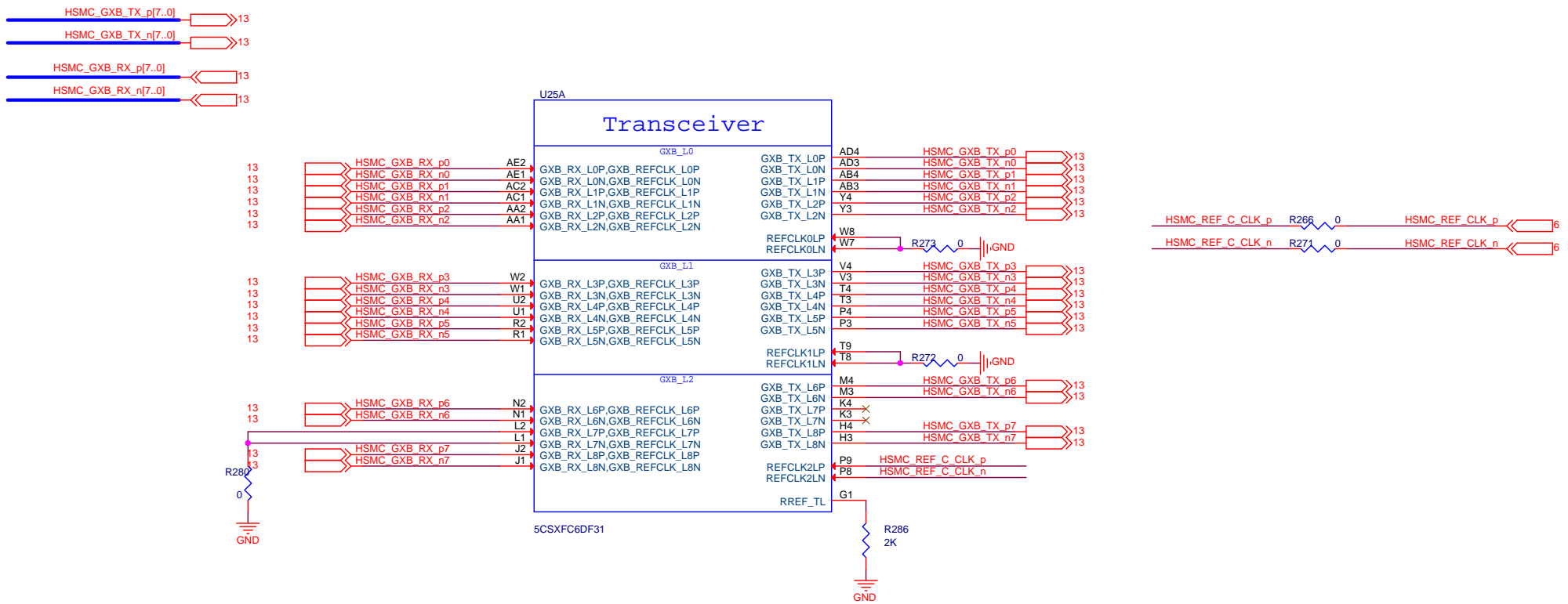
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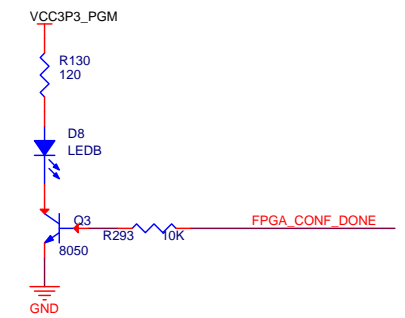
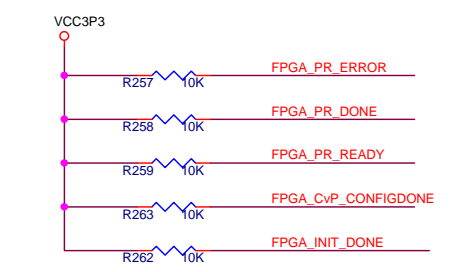
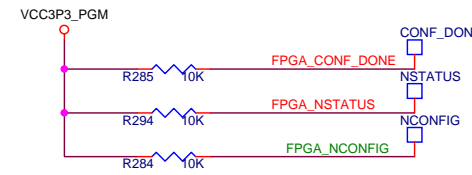
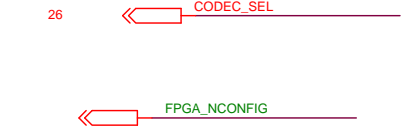
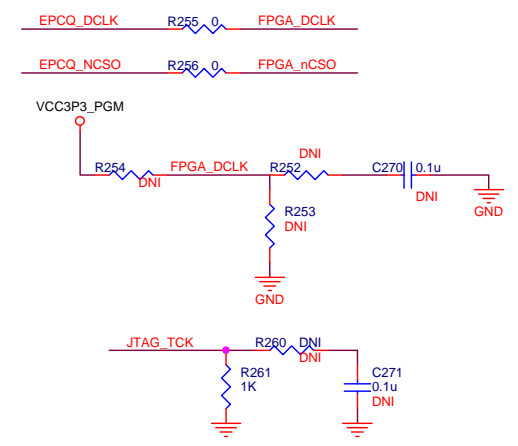
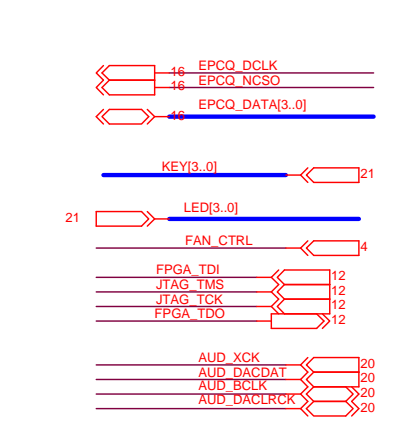
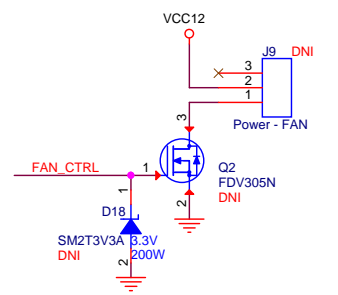
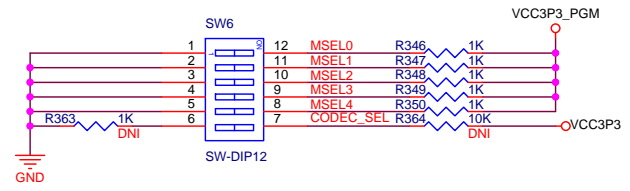
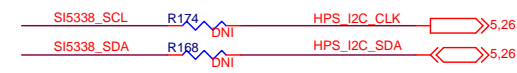
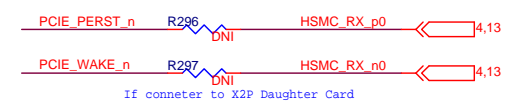
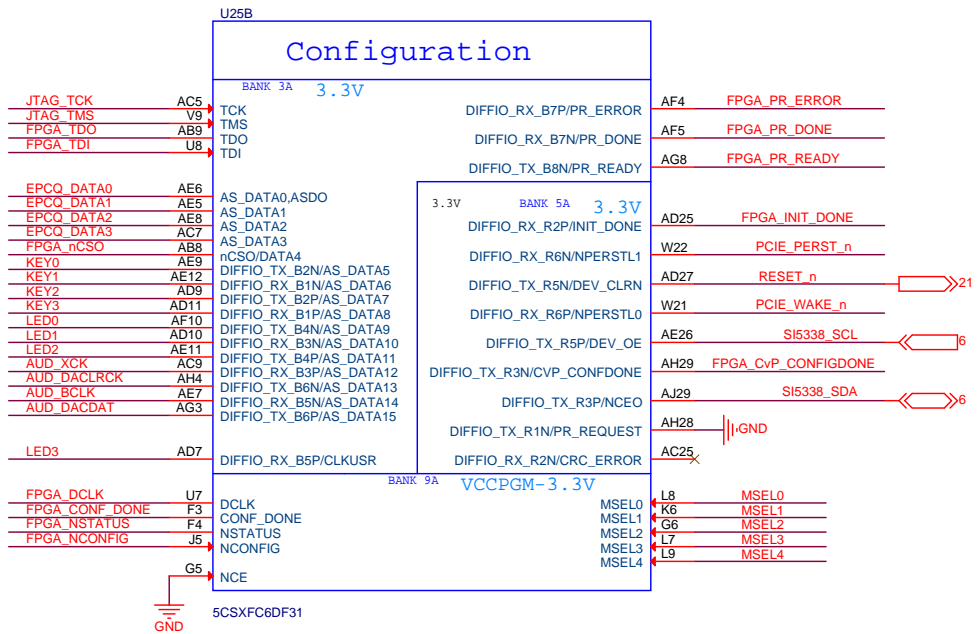


GND

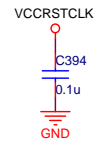
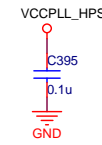
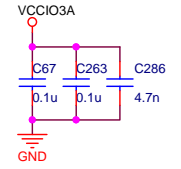
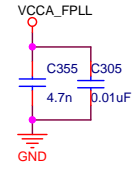
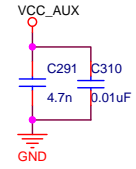
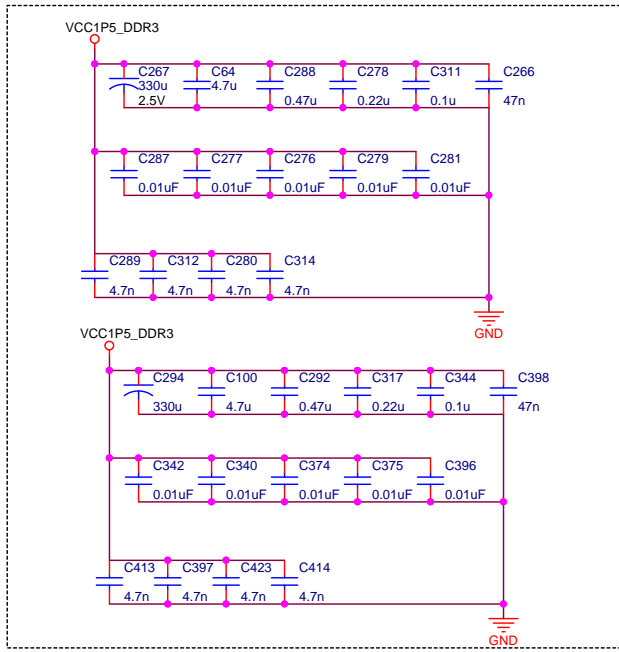
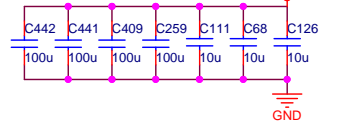
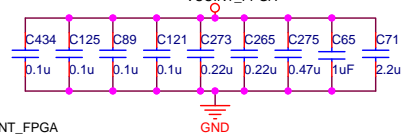
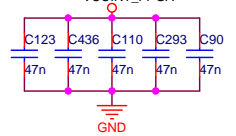
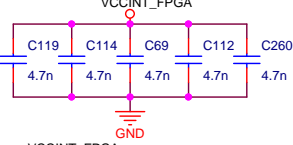
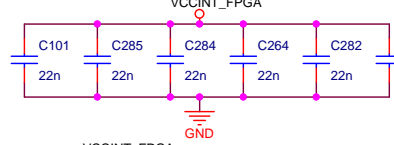
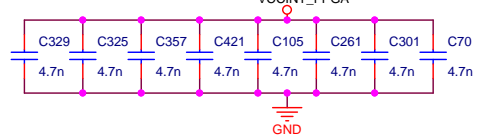
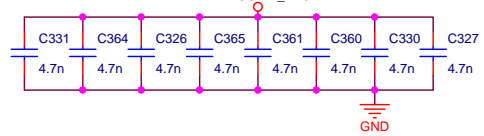
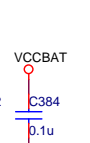
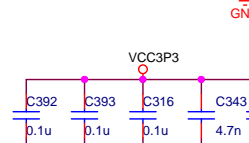
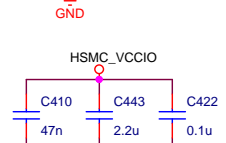
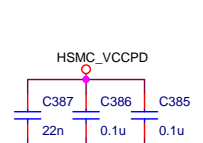
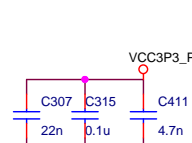
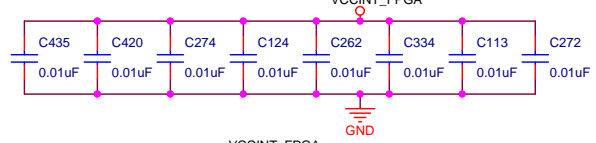
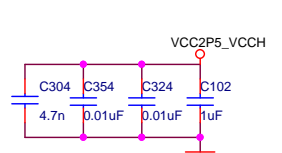
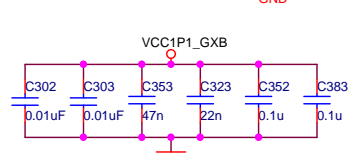
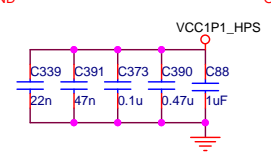
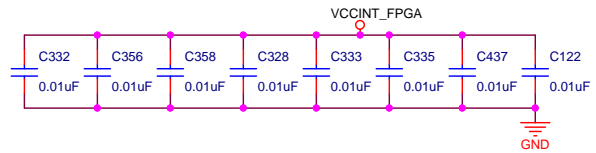
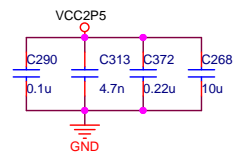
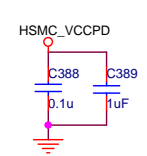
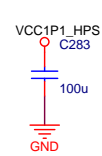
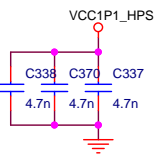
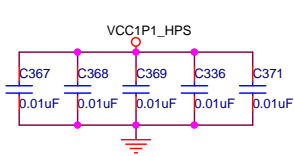
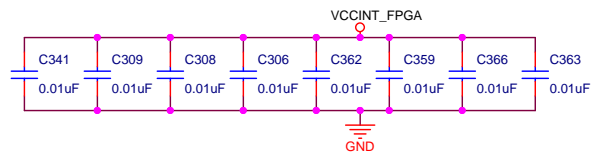
GND

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SoCKit Board		
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B	Clocks & GND	E
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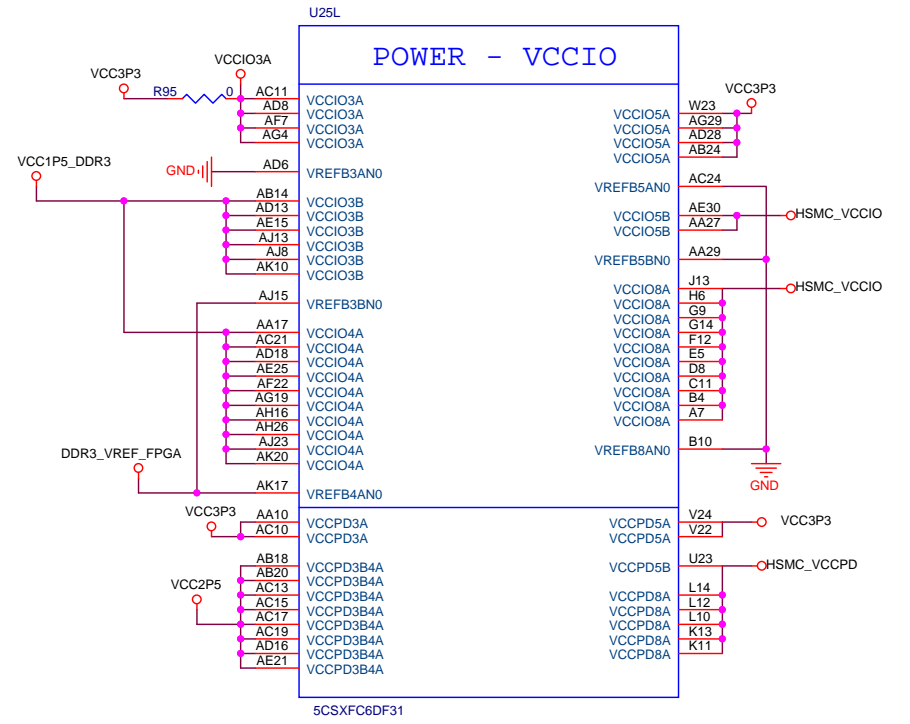
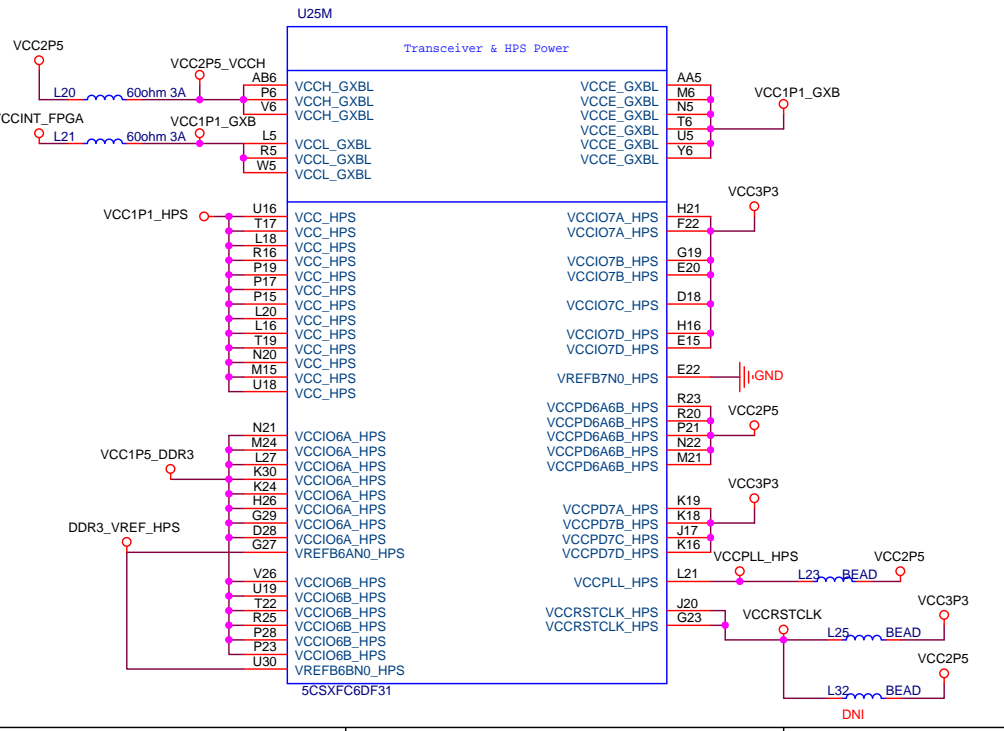
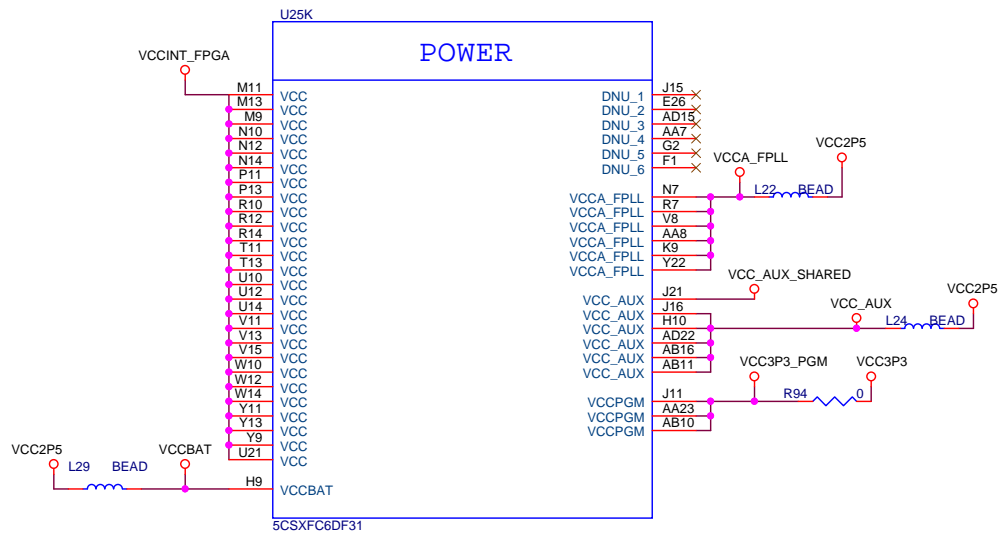




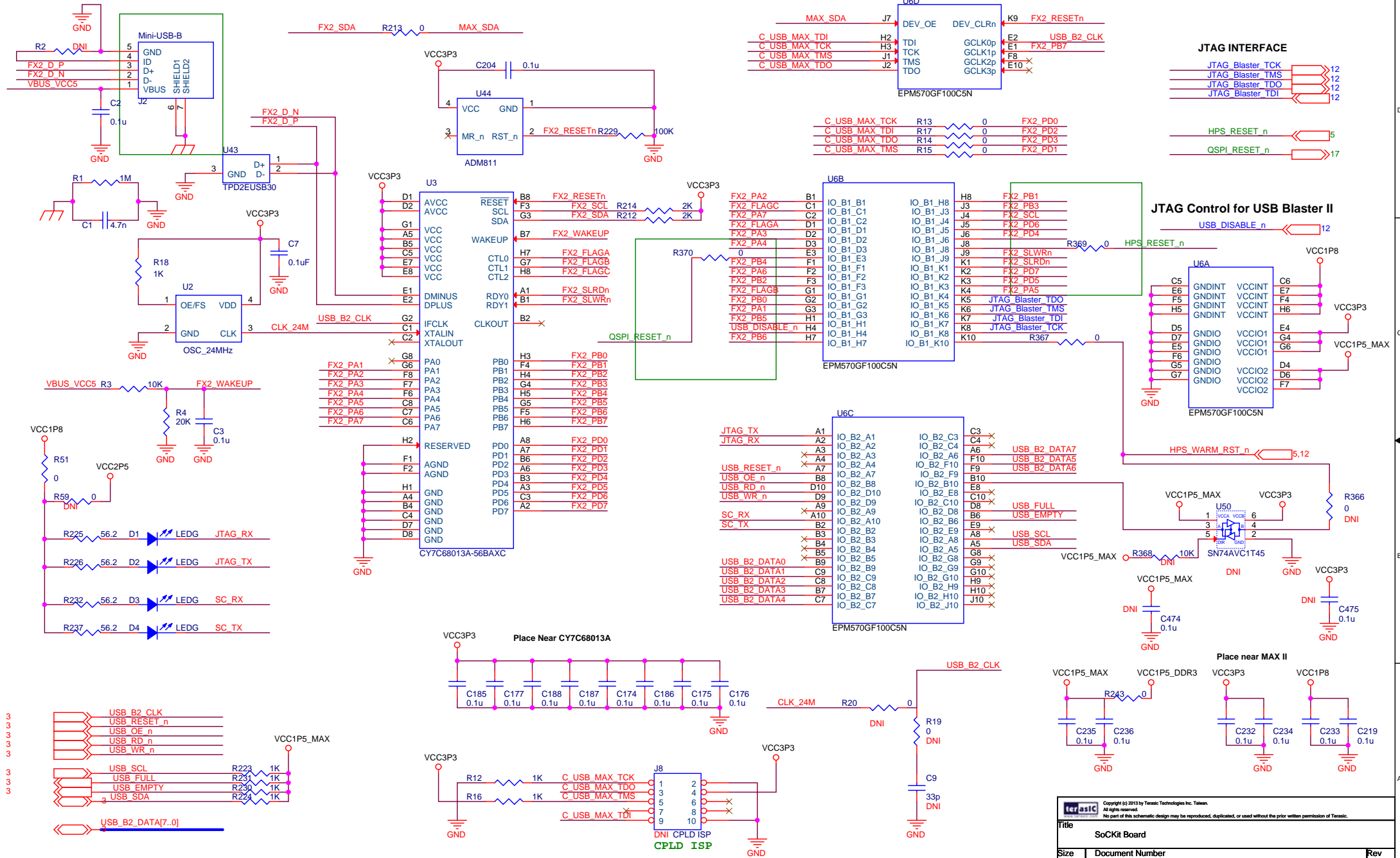
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Size B	Document Number: Decoupling	Rev E
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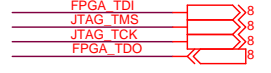


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USB Blaster



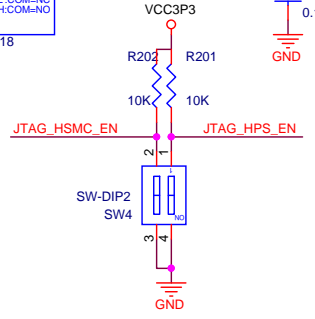
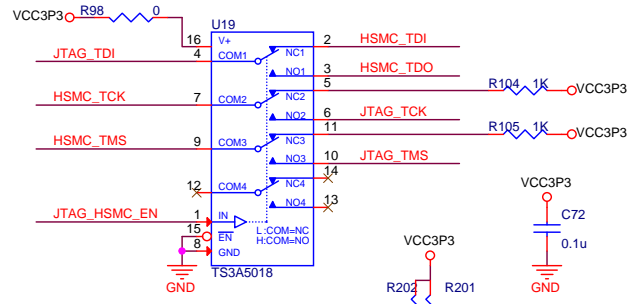
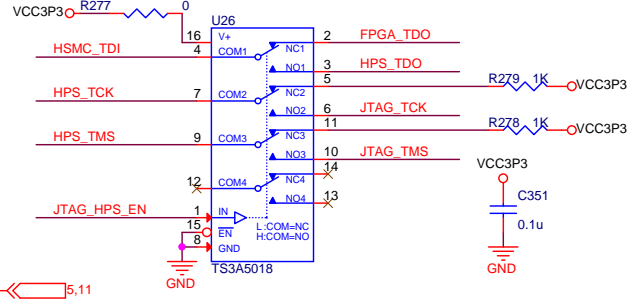
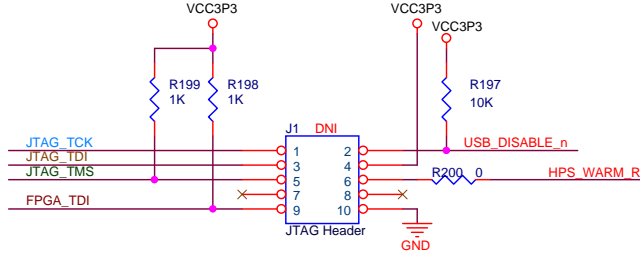
FPGA JTAG INTERFACE



HSMC JTAG INTERFACE



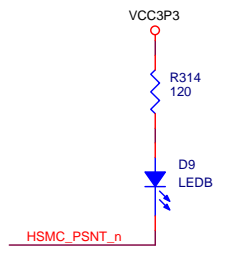
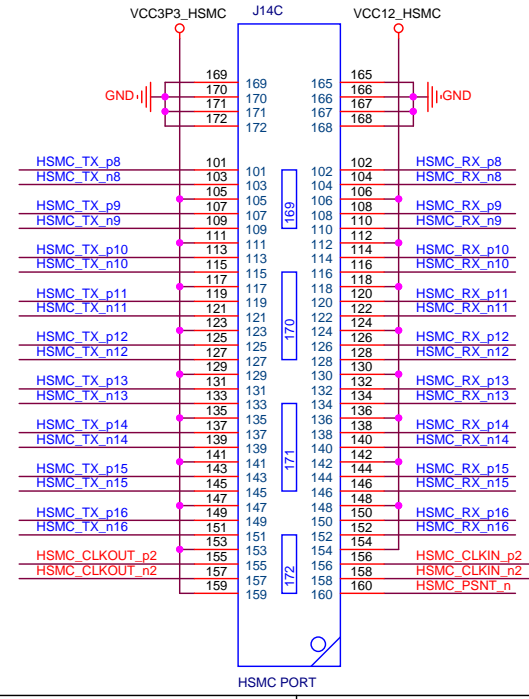
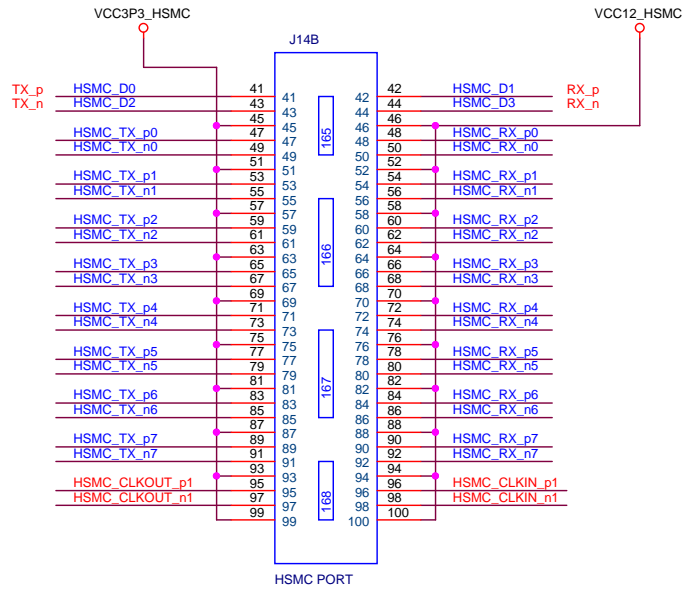
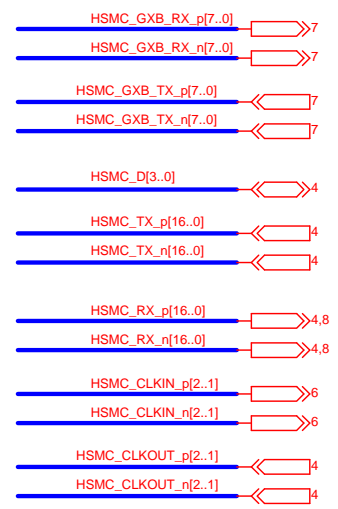
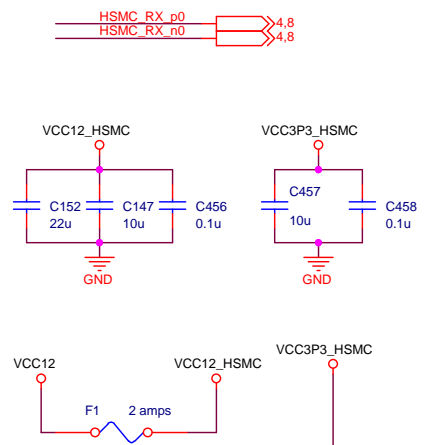
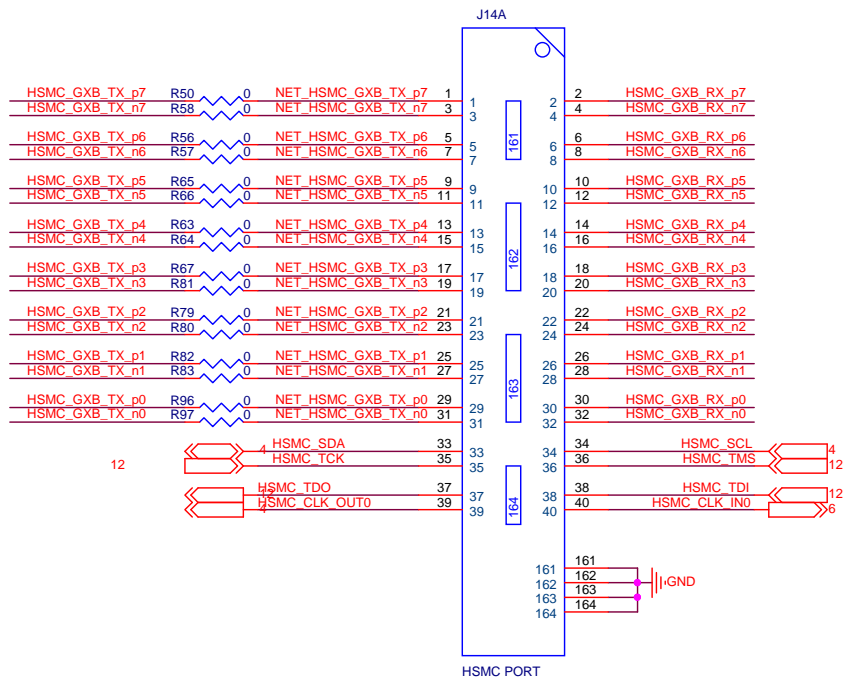
HPS JTAG INTERFACE

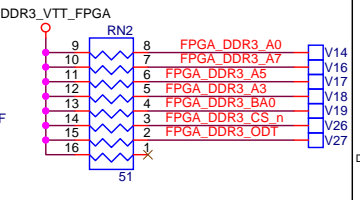
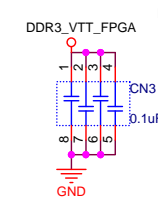
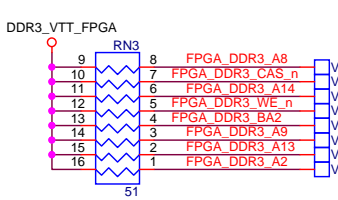
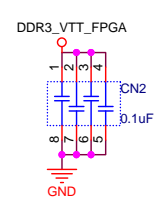
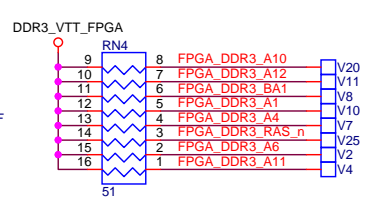
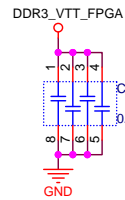
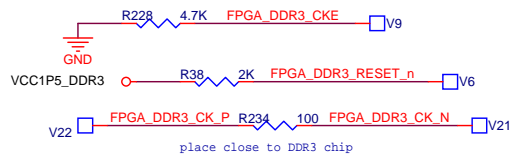


Default Disable (switch OFF)

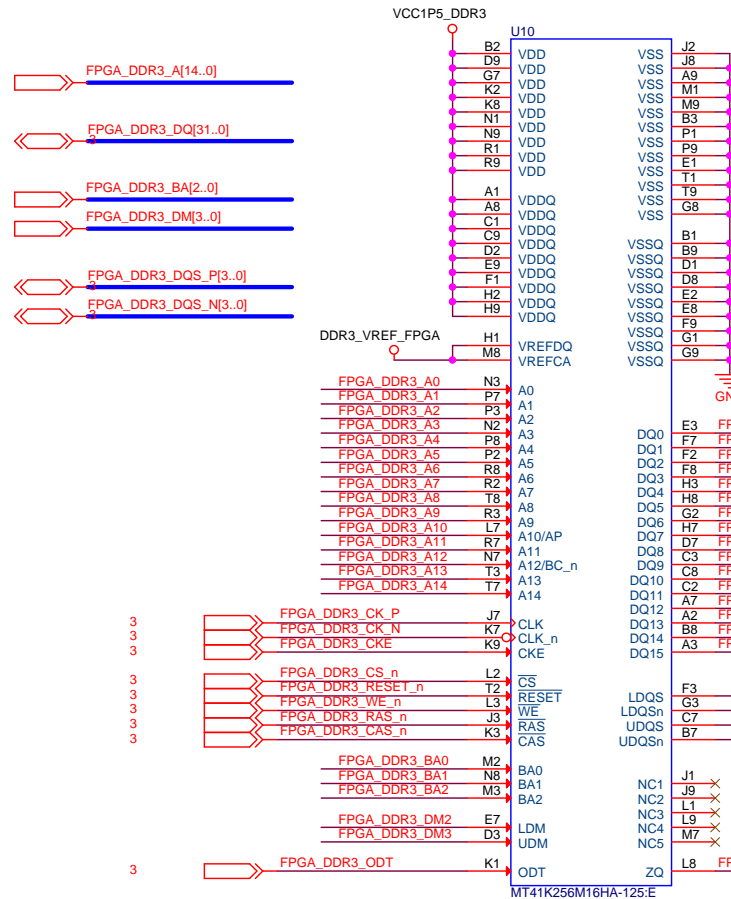
OFF = in-chain
ON = not-in-chain

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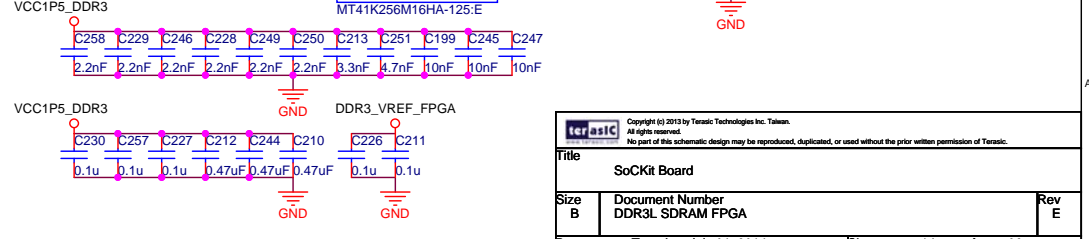
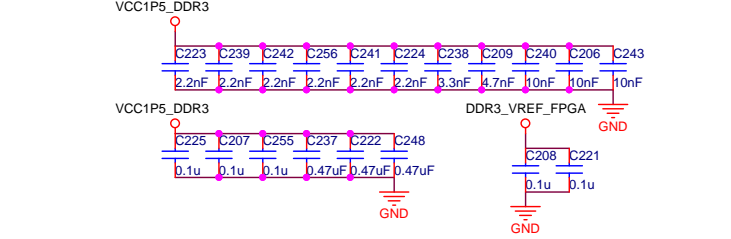




Note: you can swap the signals on the OCT resistor array (include NC pin)



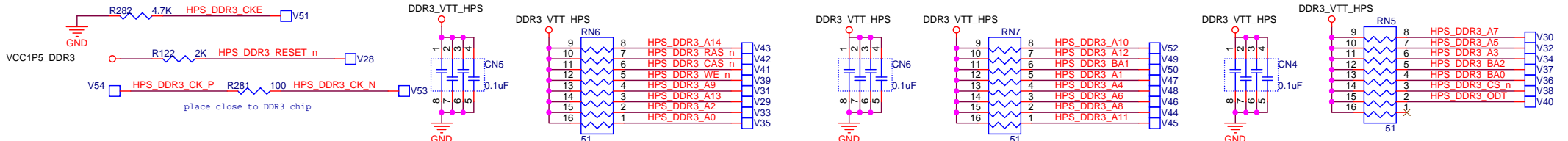
Note: you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31,32-39) on the DDR3 chips



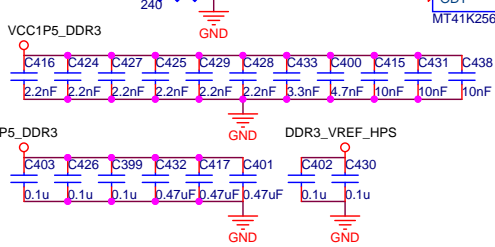
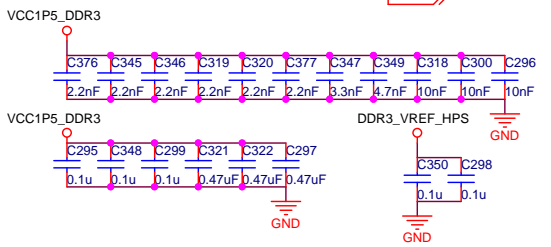
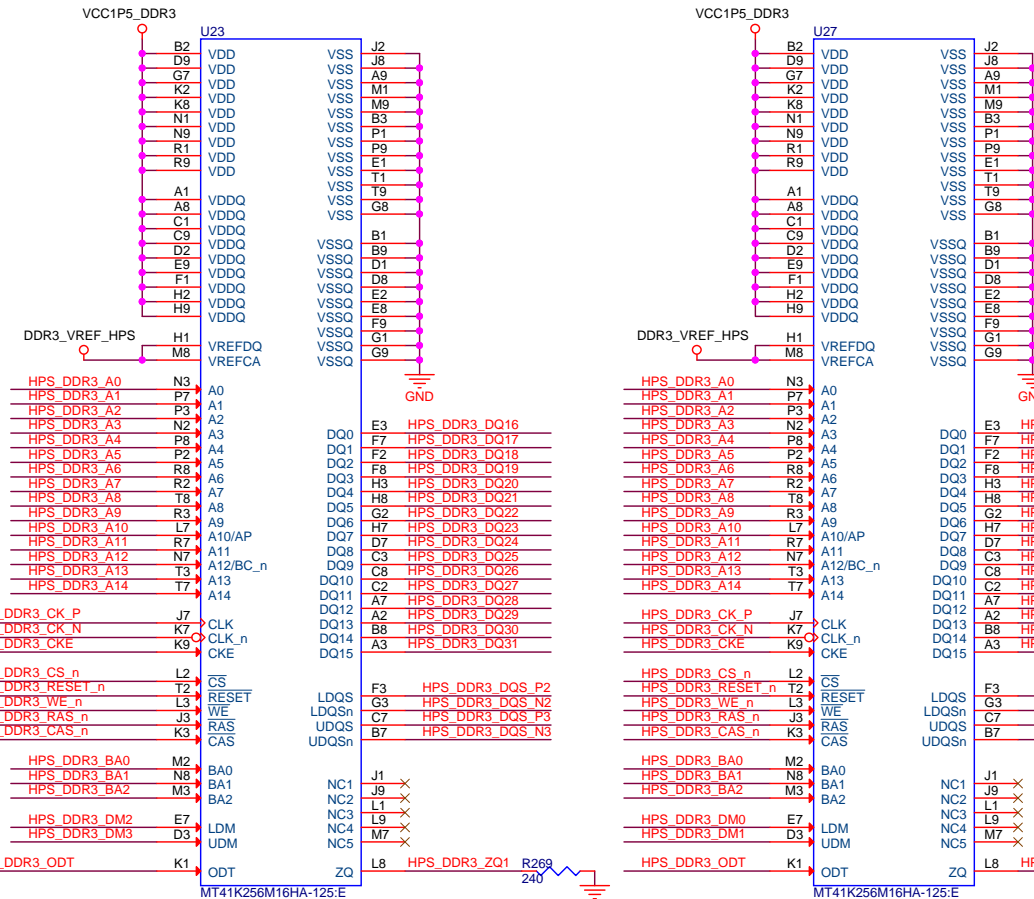
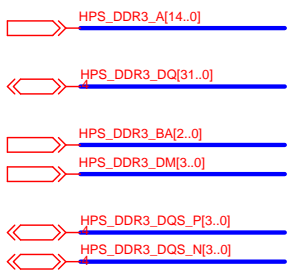
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Title
SoCKit Board

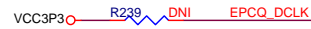
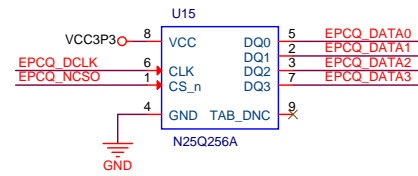
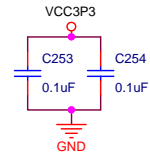
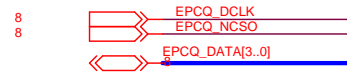
Size B	Document Number DDR3L SDRAM FPGA	Rev E
Date: Tuesday, July 01, 2014		Sheet 14 of 32




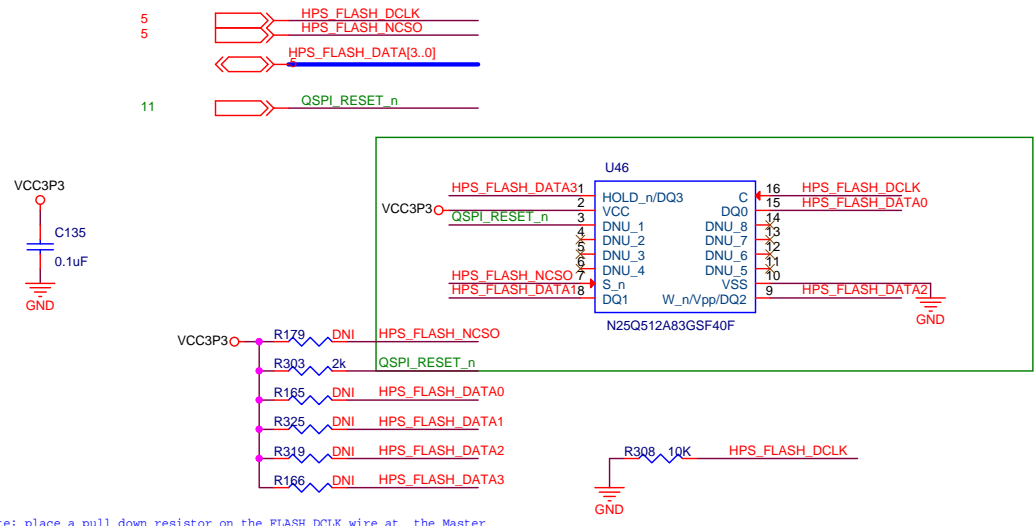
Note: you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31) on the DDR3 chips Note: you can swap the signals on the OCT resistor array(include NC pin)




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Title		
SoCKit Board		
Size	Document Number	Rev
B	DDR3L SDRAM HPS	E
Date:	Tuesday, July 01, 2014	Sheet 15 of 32

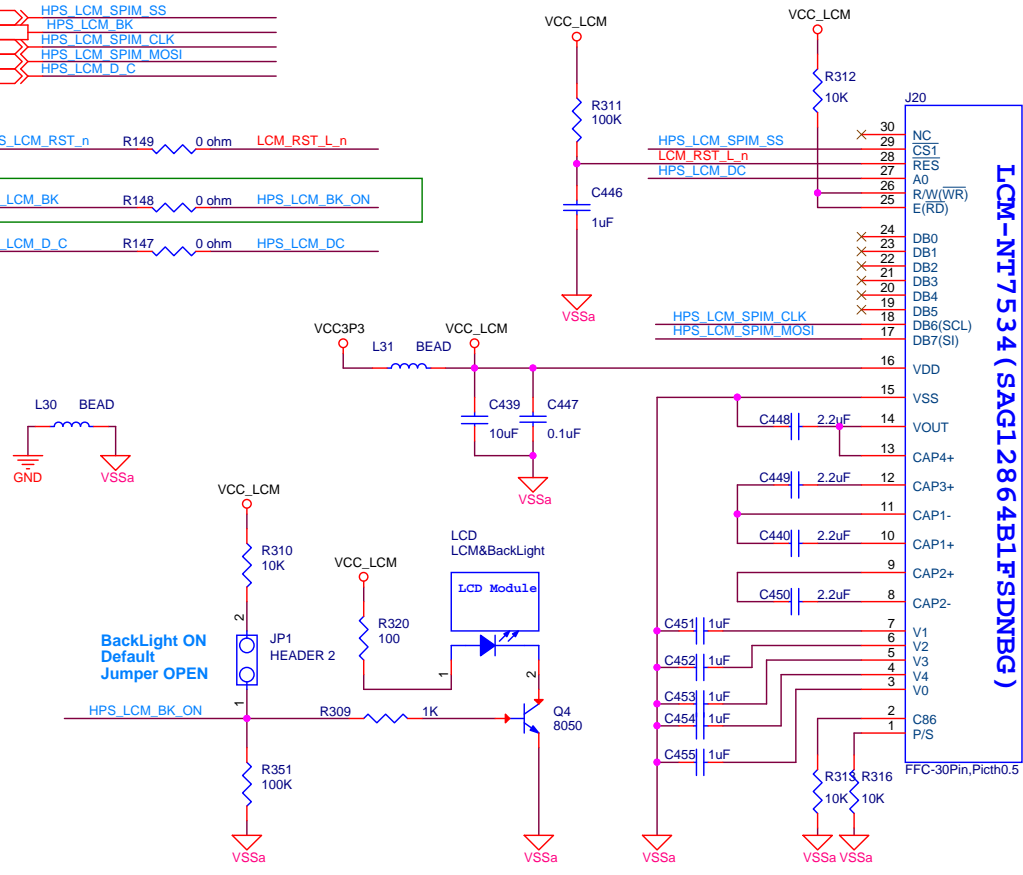
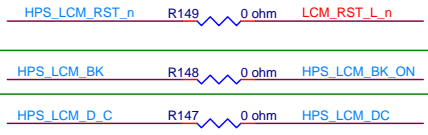
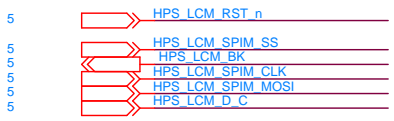


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Title	
SoCKit Board	
Size	Document Number
B	EPCQ
Date:	Tuesday, July 01, 2014
Sheet	16 of 32
Rev	E

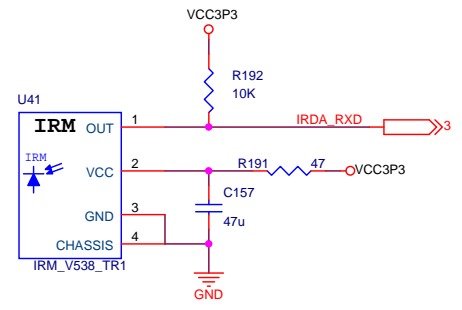
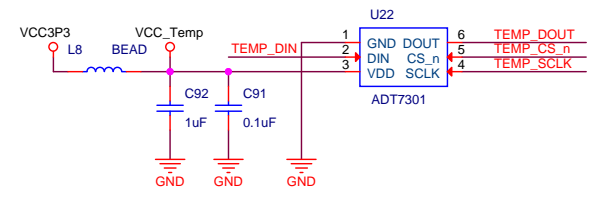
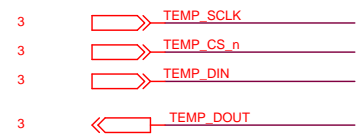


Note: place a pull down resistor on the FLASH_DCLK wire at the Master

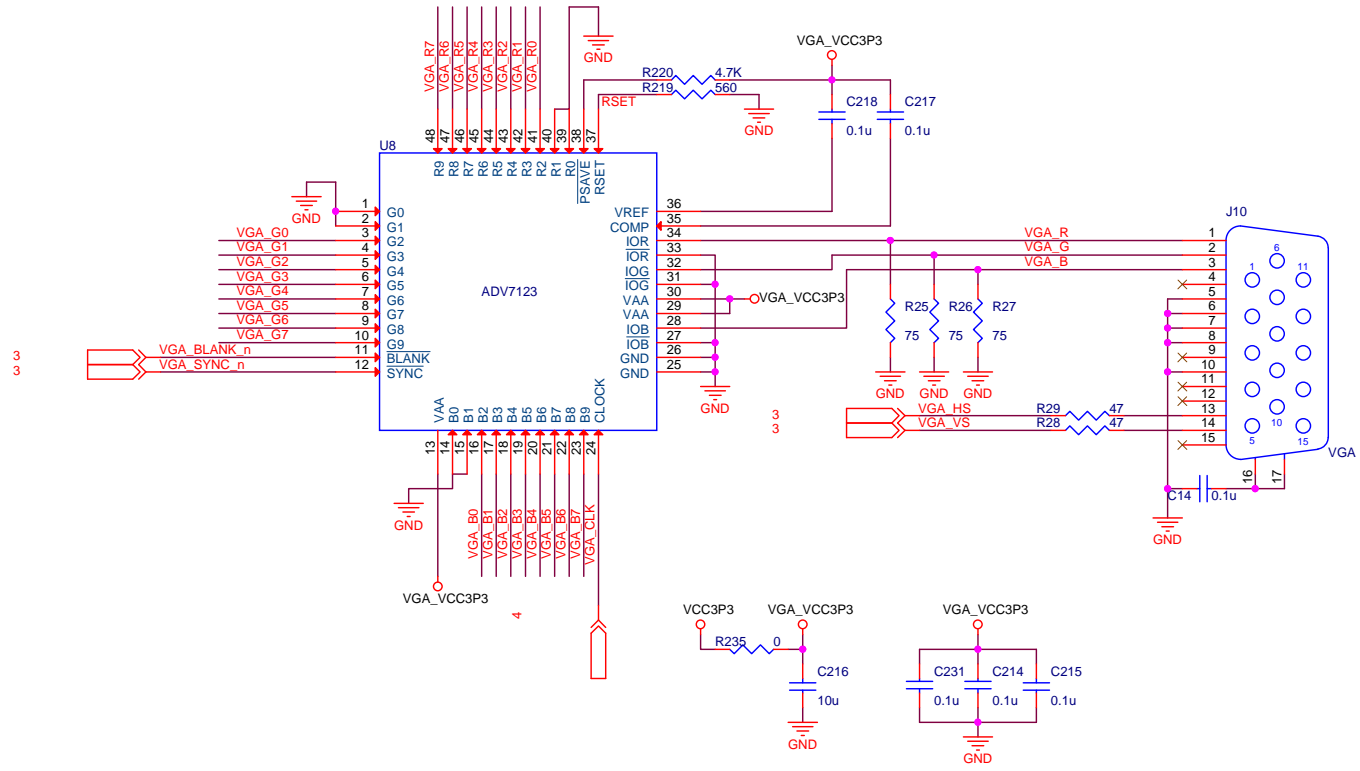
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Title	
SoCKit Board	
Size	Document Number
B	QSPI FLASH HPS
Date:	Tuesday, July 01, 2014
Sheet	17 of 32
Rev	E



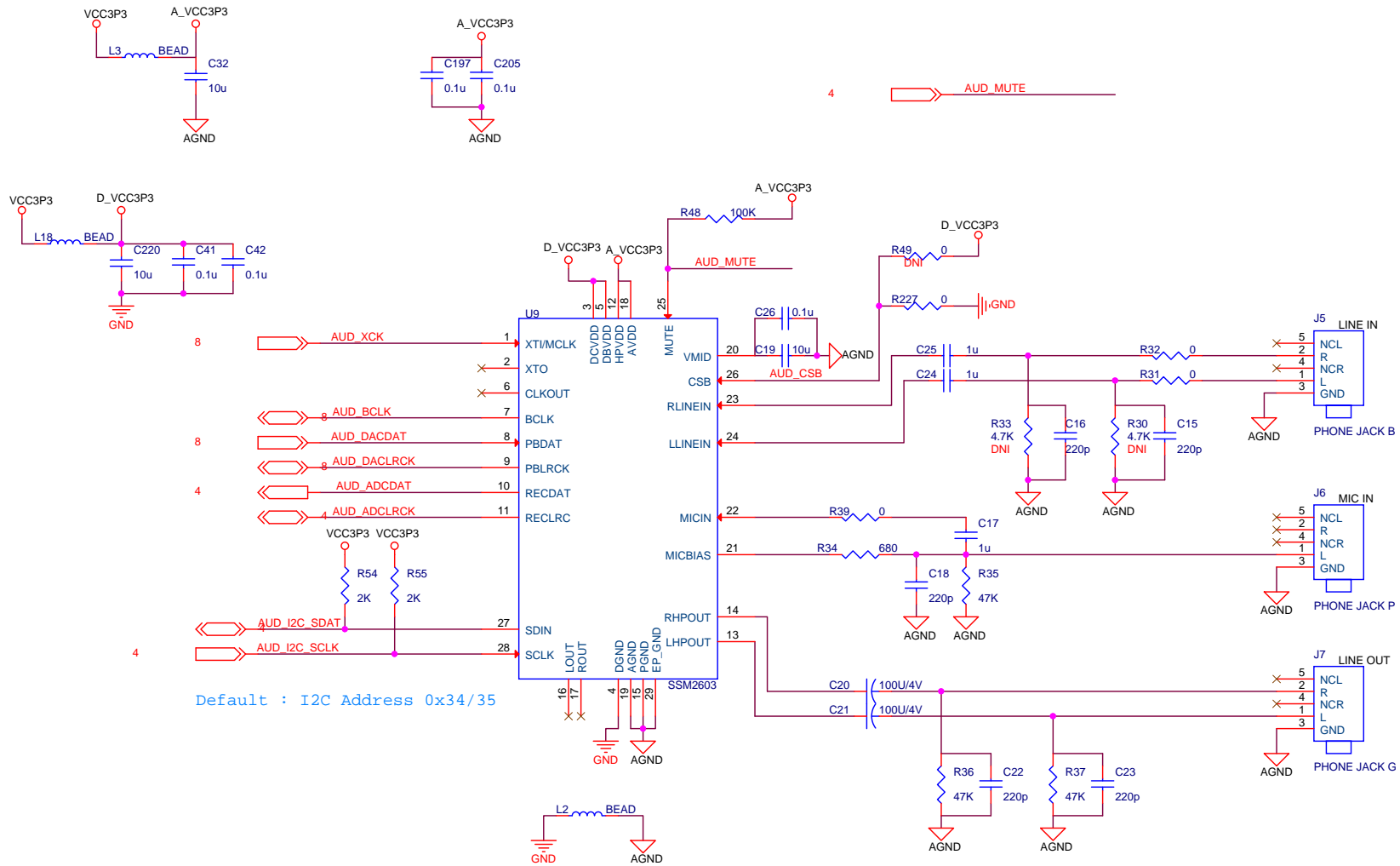
LCM-NT7534 (SAG12864B1FSDNBG)




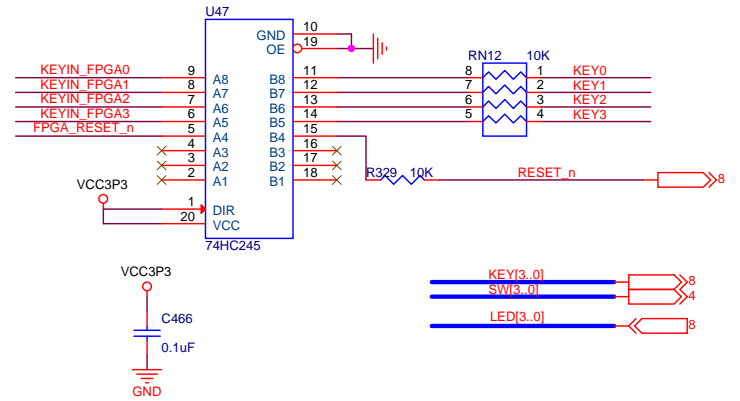
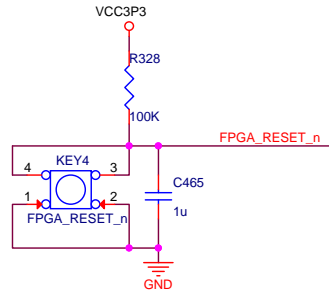
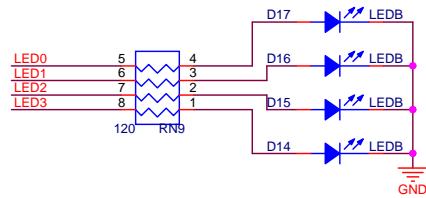
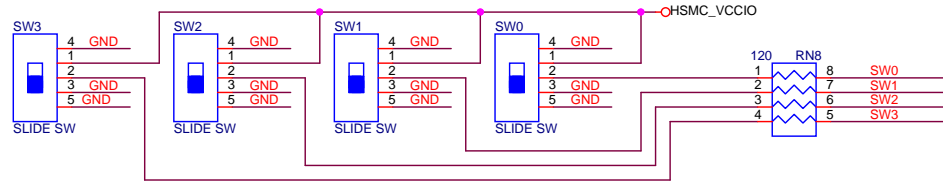
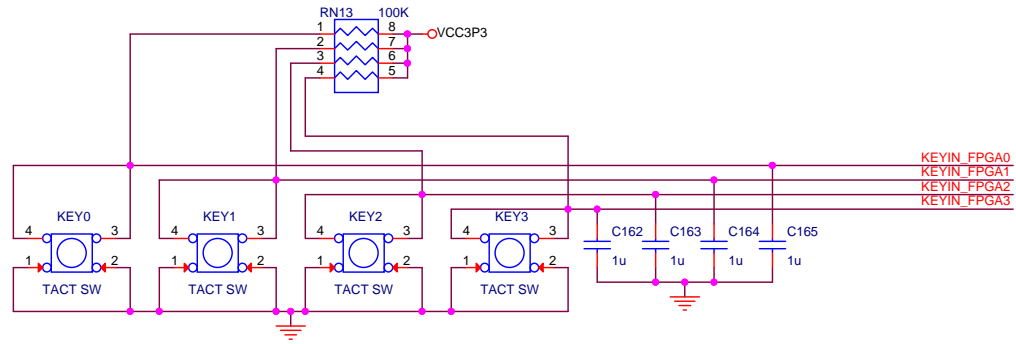
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Title		
SoCKit Board		
Size	Document Number	Rev
B	LCD & Temp sensor & IRM	E
Date:	Tuesday, July 01, 2014	Sheet 18 of 32



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Title: SoCKit Board		
Size: B	Document Number: VGA ADV7123	Rev: E
Date: Tuesday, July 01, 2014	Sheet: 19	of 32

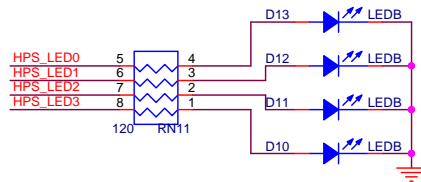
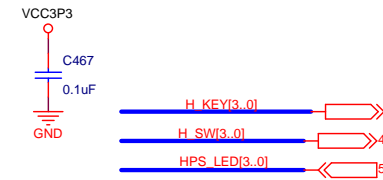
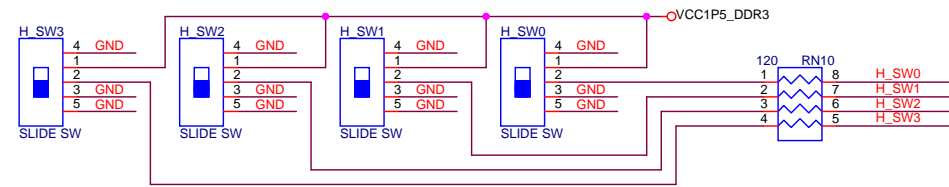
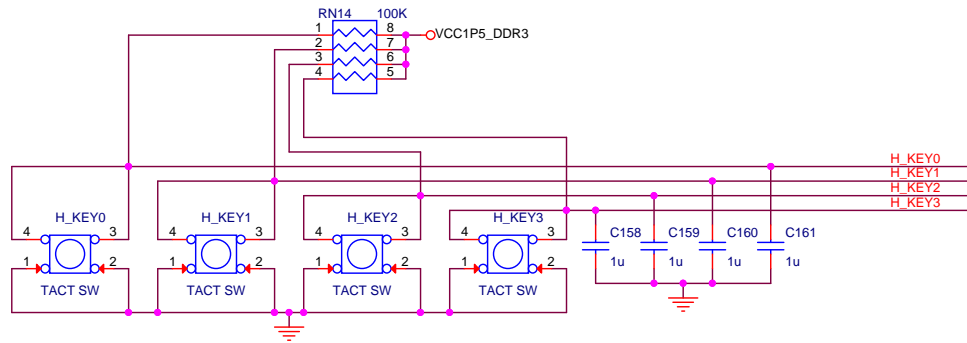


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Title		
SoCKit Board		
Size	Document Number	Rev
B	Audio DAC	E
Date:	Tuesday, July 01, 2014	Sheet 20 of 32



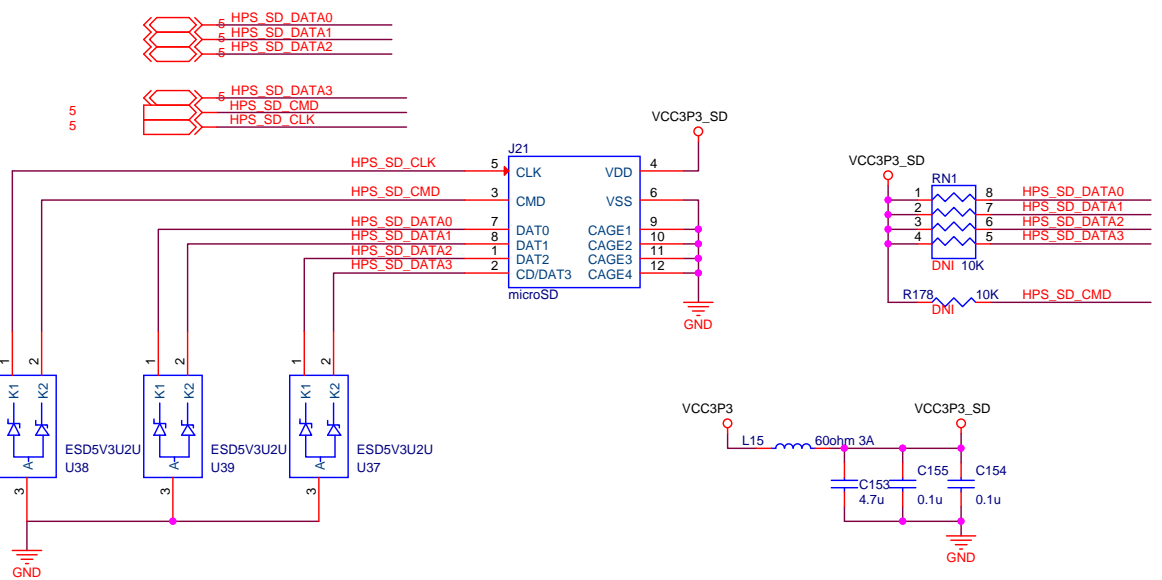
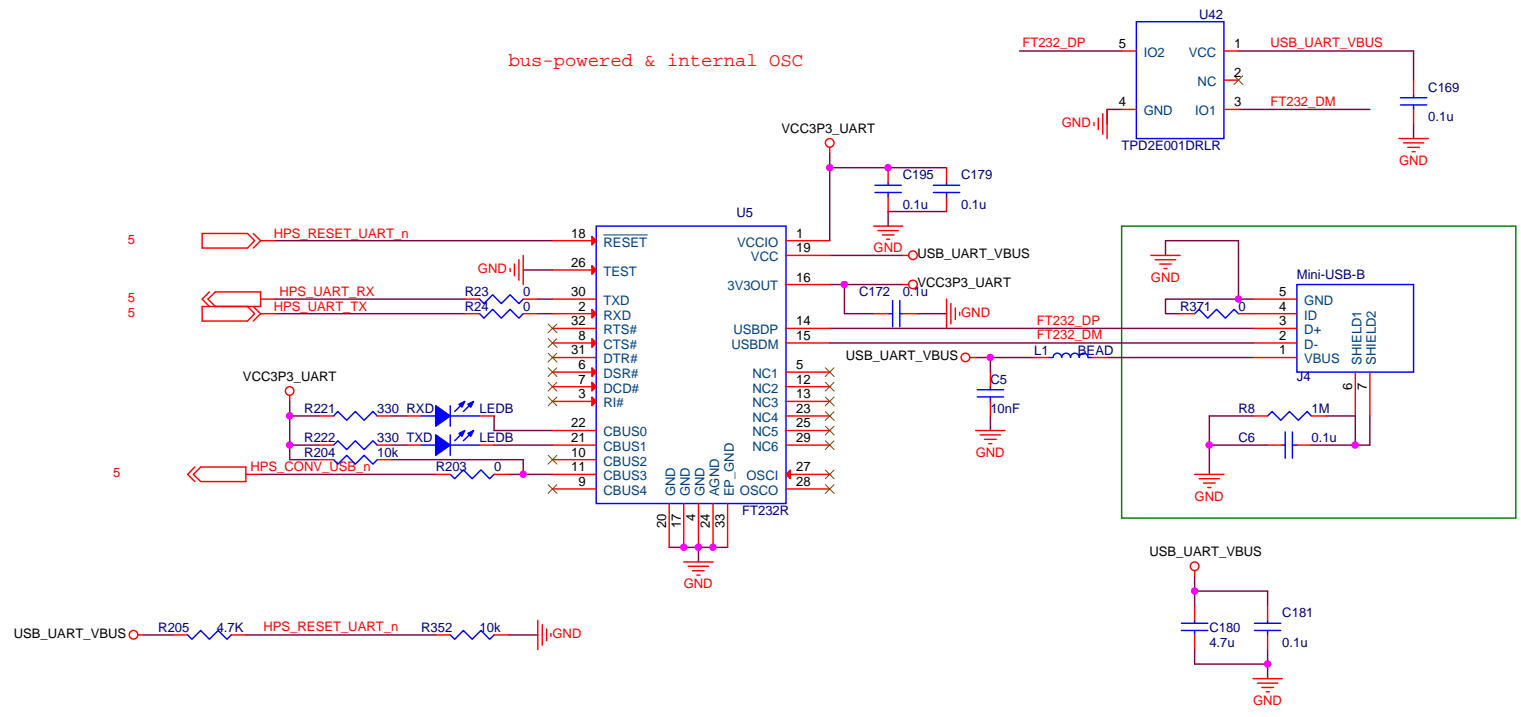
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Title		
SoCKit Board		
Size B	Document Number	Rev E
FPGA BUTTON & SW		
Date:	Tuesday, July 01, 2014	Sheet 21 of 32

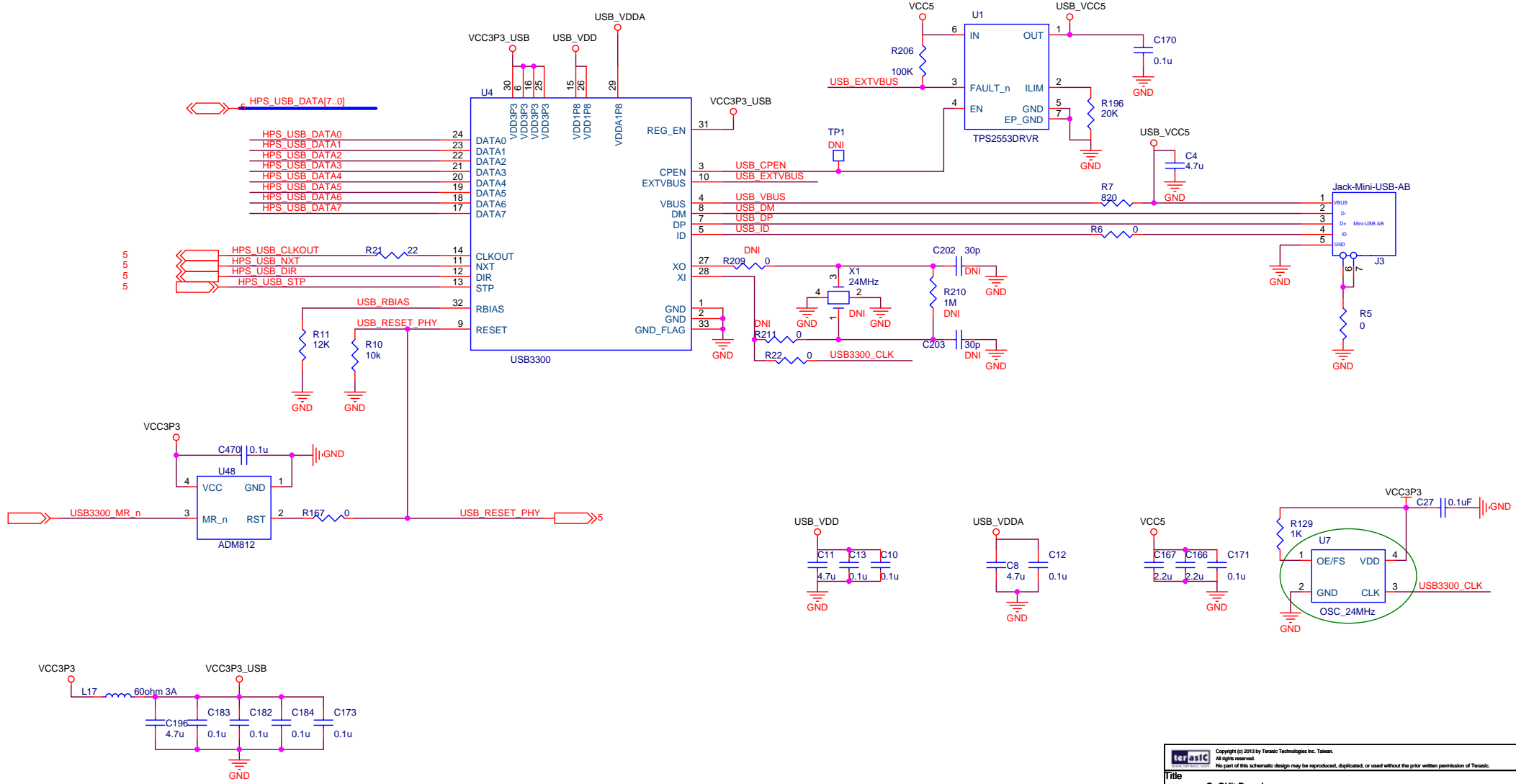


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Title	
SoCKit Board	
Size	Document Number
B	HPS BUTTON & SW
Date:	Rev
Tuesday, July 01, 2014	E
Sheet	22 of 32
1	

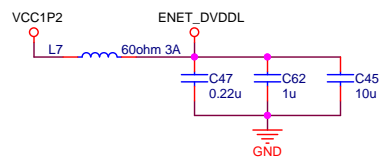
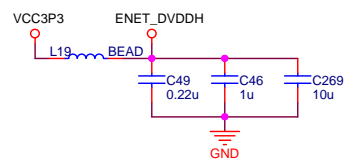
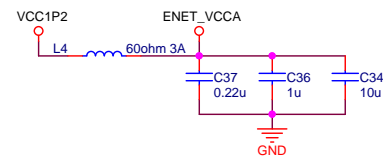
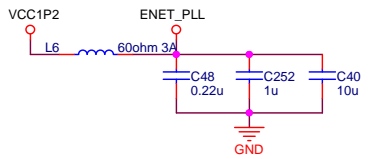
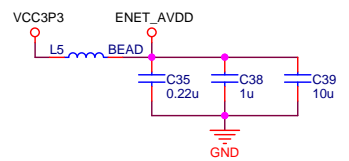
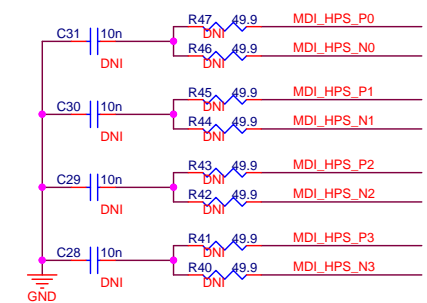
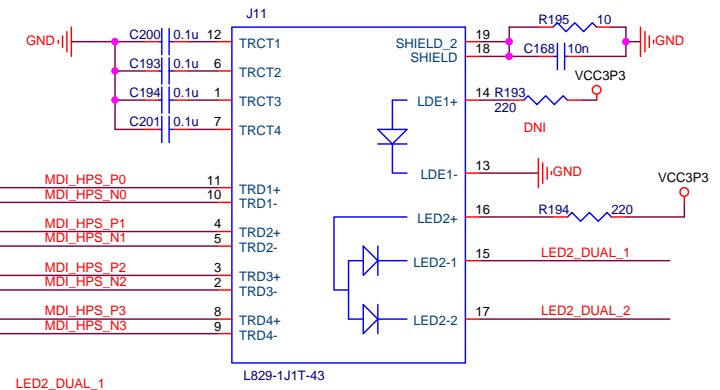
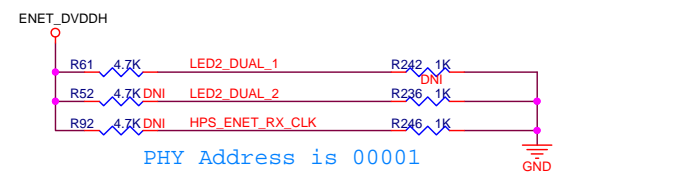
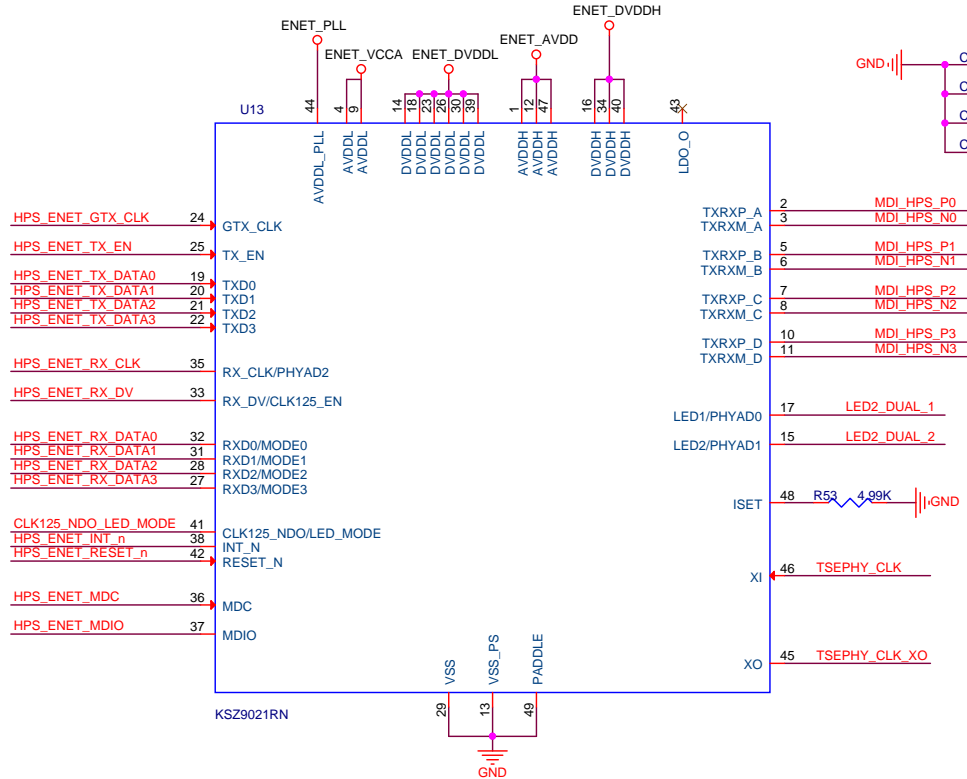
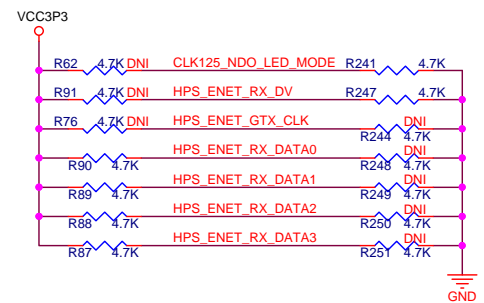
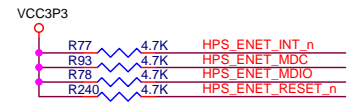
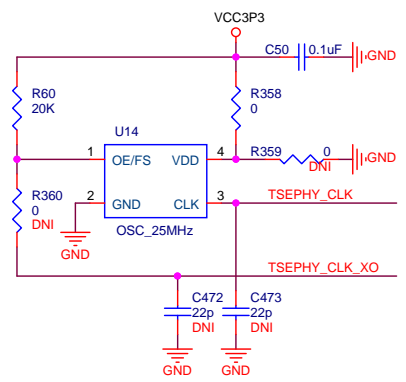
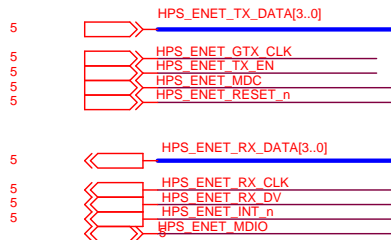
bus-powered & internal OSC



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Title		
SoCKit Board		
Size	Document Number	Rev
B	USB to UART & SD CARD	E
Date:	Tuesday, July 01, 2014	Sheet 23 of 32



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Title		
SoCKit Board		
Size	Document Number	Rev
B	USB3300	E
Date:	Tuesday, July 01, 2014	Sheet 24 of 32

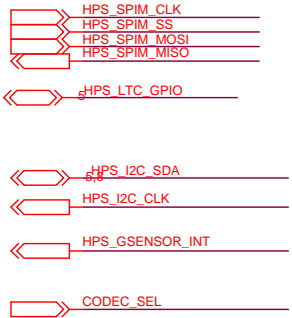


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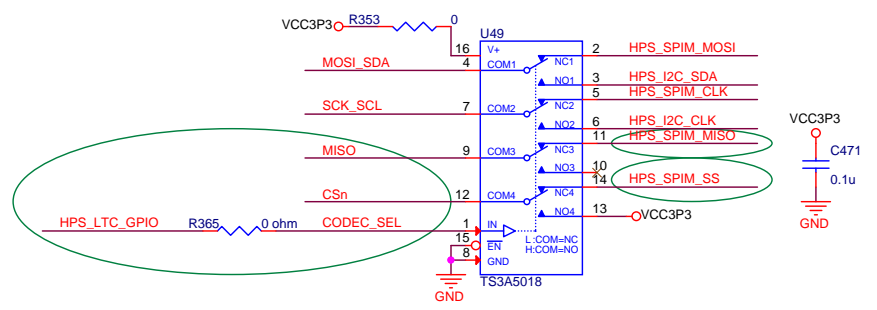
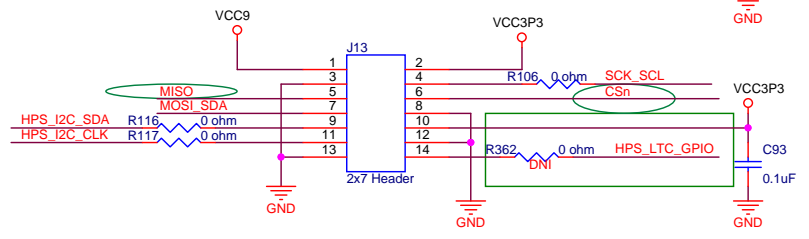
Title SoCKit Board

Size B	Document Number TSE PHY	Rev E
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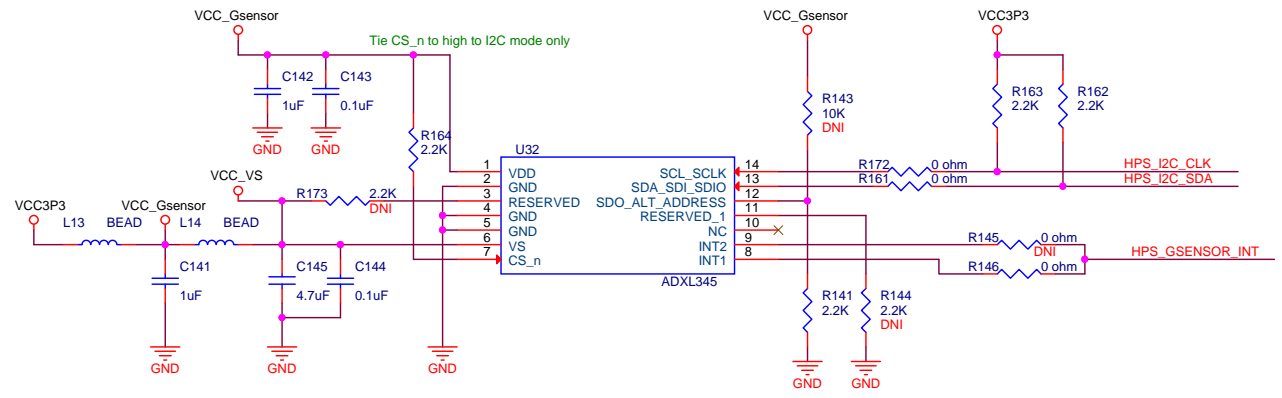
Date: Tuesday, July 01, 2014 Sheet 25 of 32



LTC 2x7 Connector

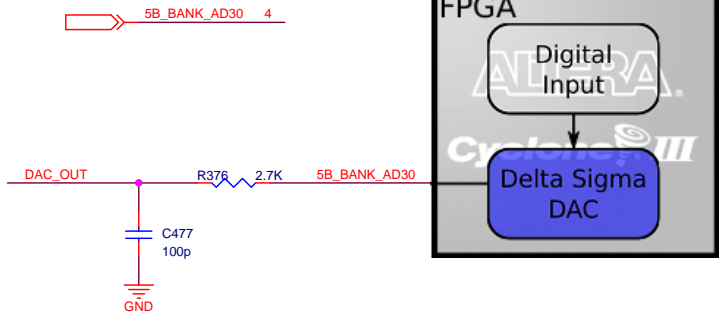
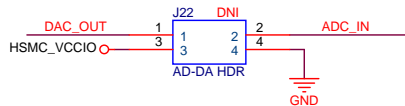
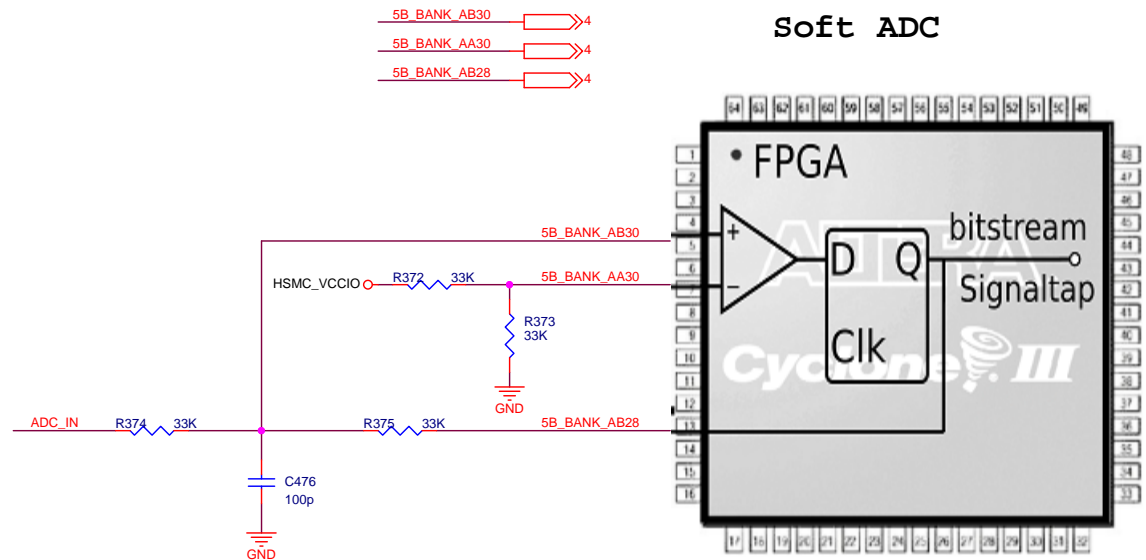



Digital Accelerometer

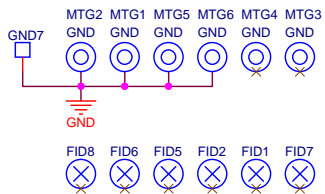


Default : I2C Address 0xA6/0xA7

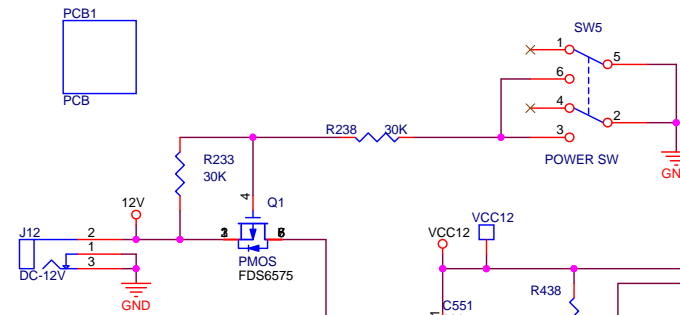
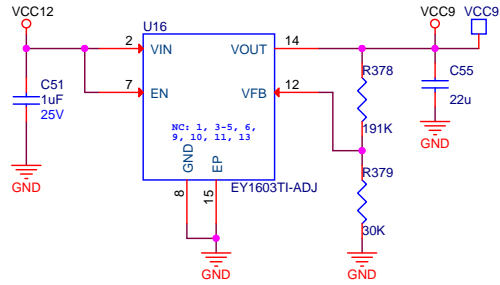
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Title		
SoCKit Board		
Size	Document Number	Rev
B	LTC Connector & G sensor	E
Date:	Tuesday, July 01, 2014	Sheet 26 of 32



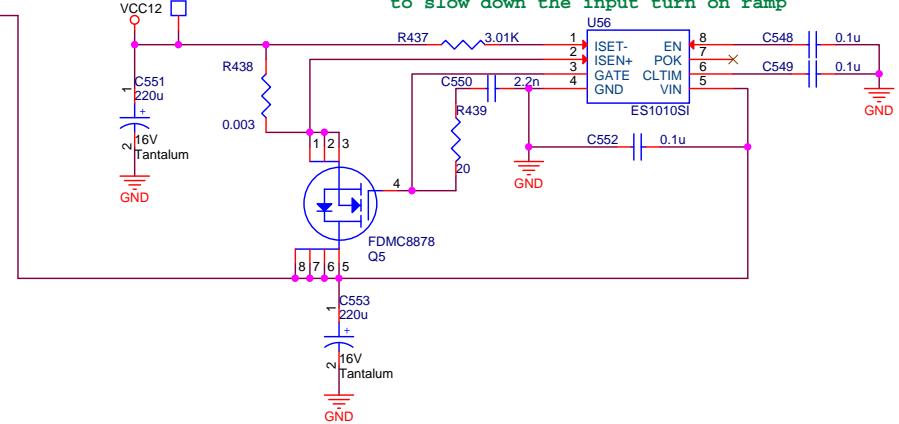
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Title		
SoCKit Board		
Size	Document Number	Rev
B	Soft ADC & DAC	E
Date:	Tuesday, July 01, 2014	Sheet 27 of 32



9V / 150mA

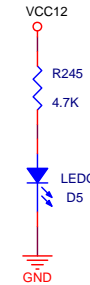
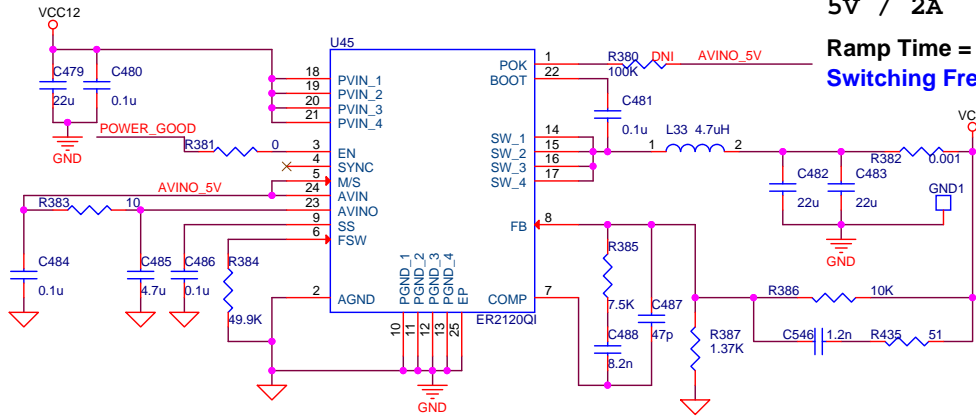


Input voltage slew rate limiting circuit to slow down the input turn on ramp



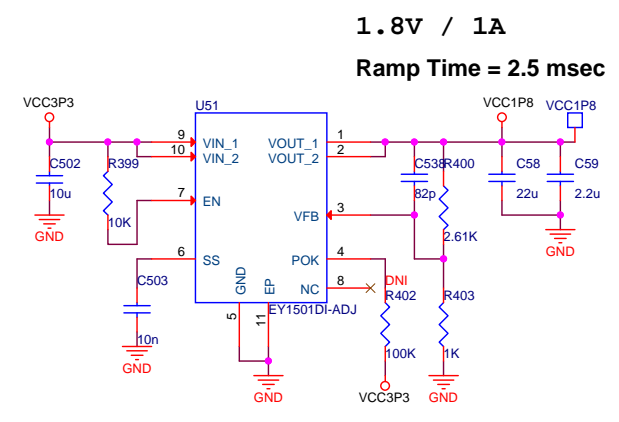
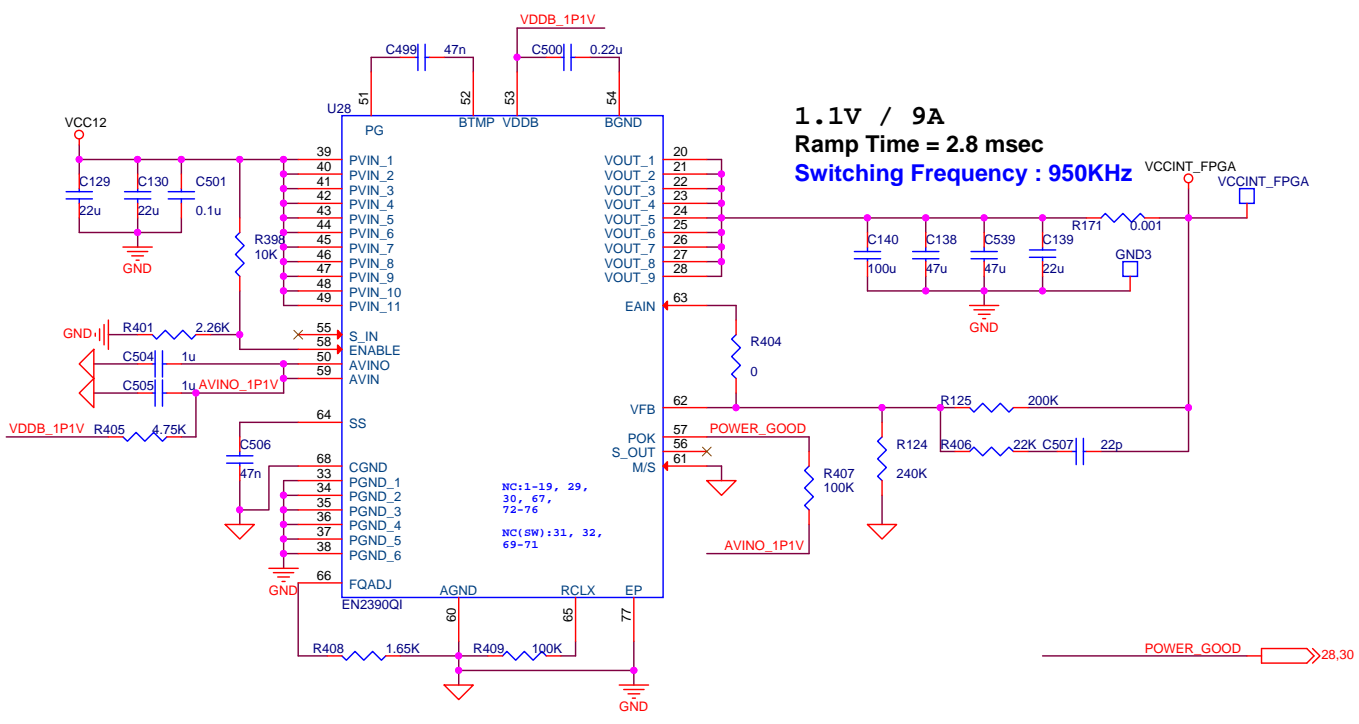
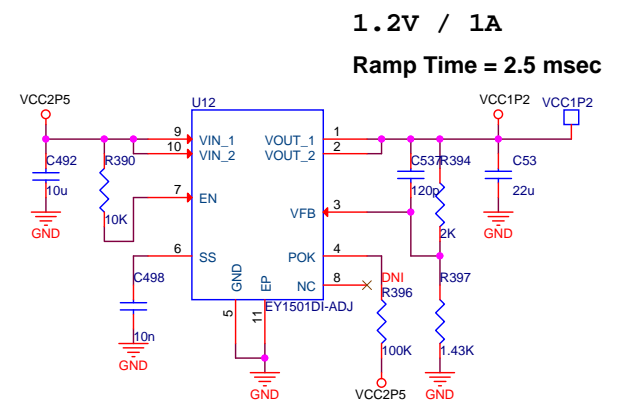
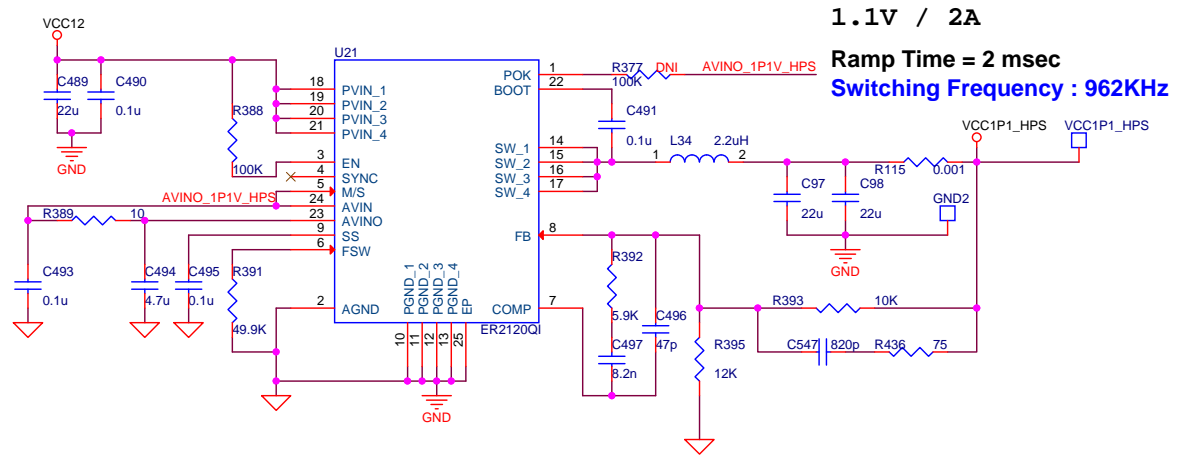
5V / 2A

Ramp Time = 2 msec
Switching Frequency : 962KHz



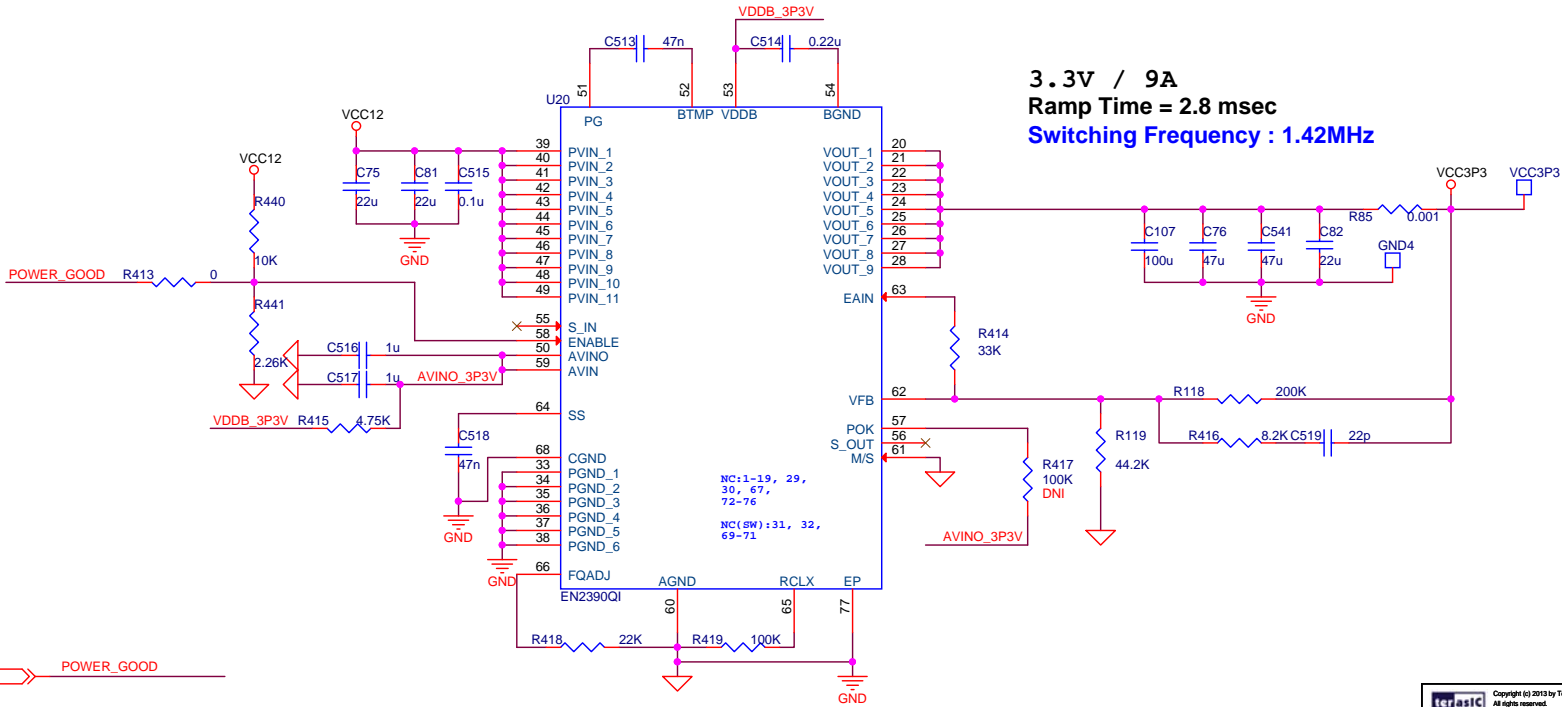
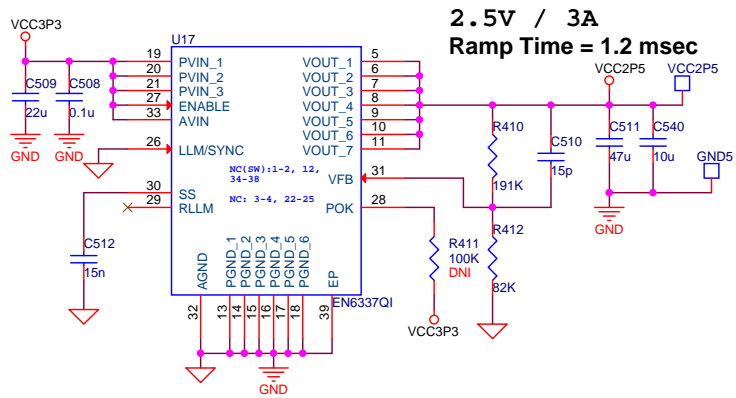
29,30 POWER_GOOD

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Title		
SoCKit Board		
Size	Document Number	Rev
B	Power - 9V & 5V	E
Date:	Tuesday, July 01, 2014	Sheet 28 of 32



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Title		
SoCKit Board		
Size	Document Number	Rev
B	Power - 1.1V & 1.2V & 1.8V	E
Date:	Tuesday, July 01, 2014	Sheet 29 of 32

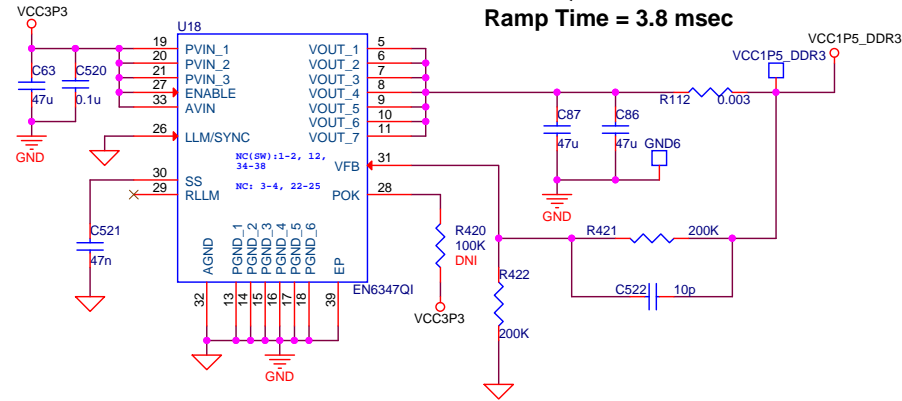


28,29 POWER_GOOD

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Title		
SoCKit Board		
Size	Document Number	Rev
B	Power - 3.3V & 2.5V	E
Date:	Tuesday, July 01, 2014	Sheet 30 of 32

DDR3L VDD,VDDQ

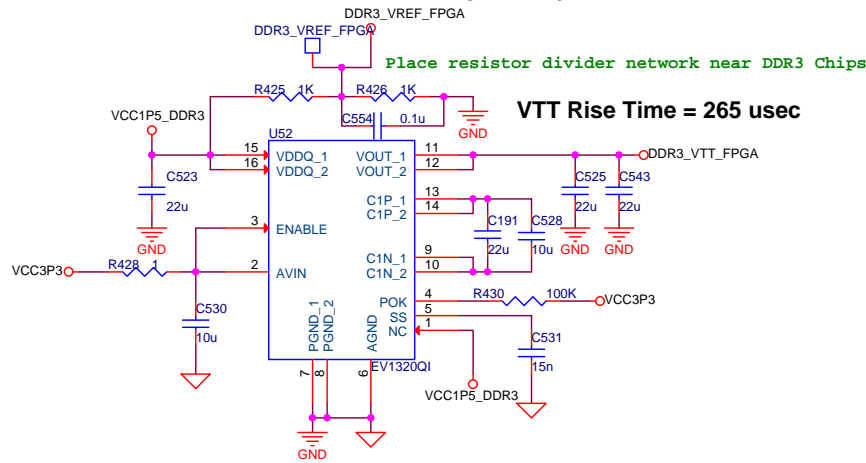
1.5V / 4A
Ramp Time = 3.8 msec



DDR3L VTT, VREF(FPGA)

Place resistor divider network near DDR3 Chips

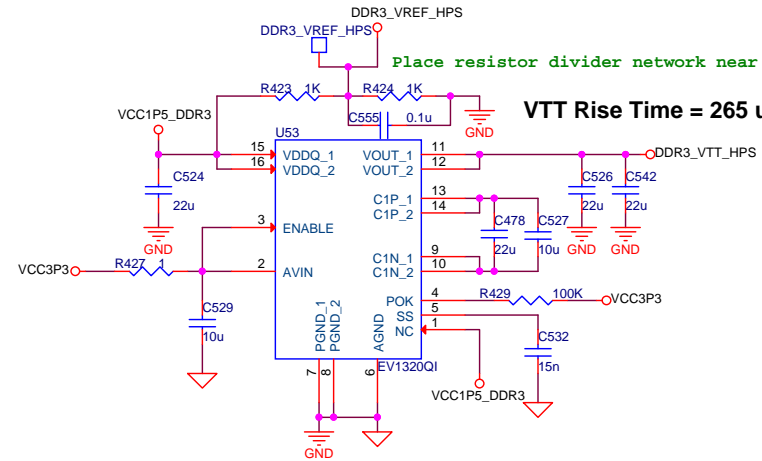
VTT Rise Time = 265 usec



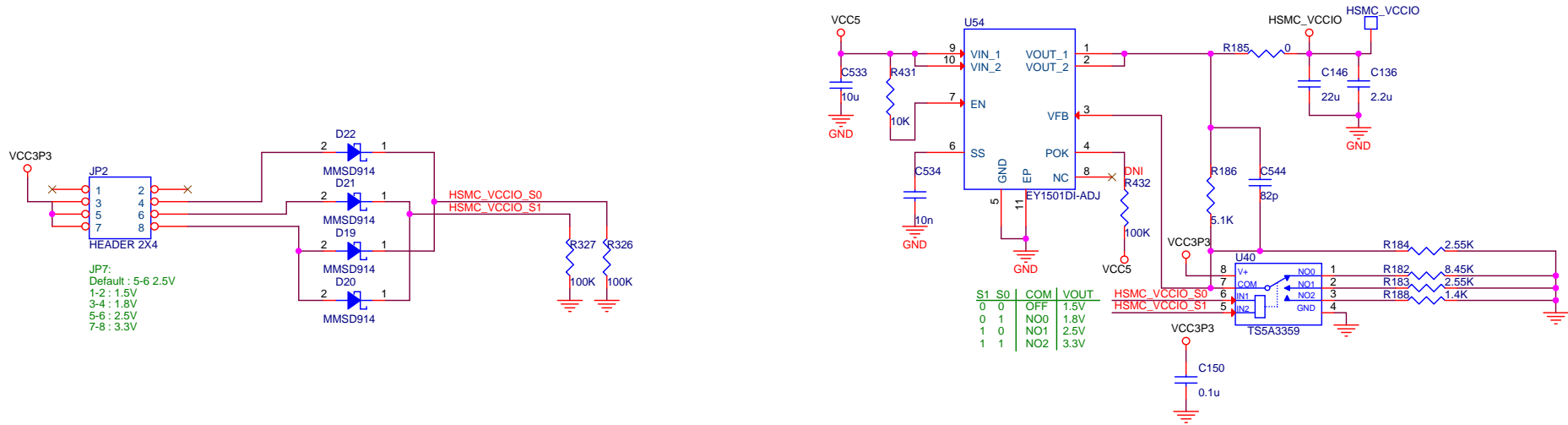
DDR3L VTT, VREF(HPS)

Place resistor divider network near DDR3 Chips

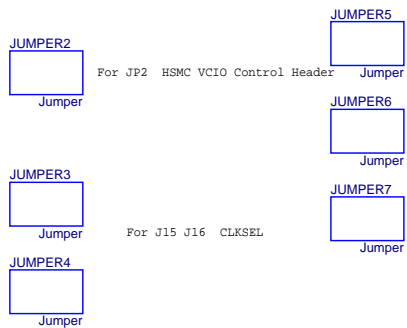
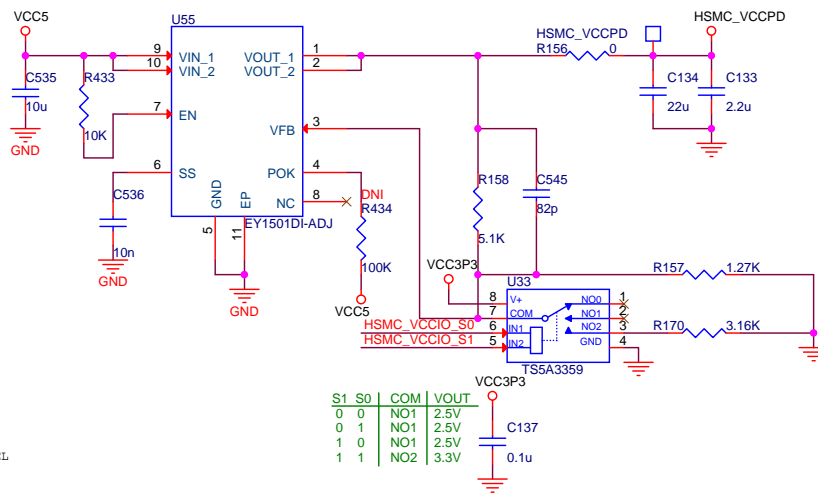
VTT Rise Time = 265 usec



HSMC_VCCIO / 1A Ramp Time = 2.5 msec



HSMC_VCCPD / 0.5A



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Title		
SoCKit Board		
Size B	Document Number Power - VCCIO_HSMC	Rev E
Date:	Tuesday, July 01, 2014	Sheet 32 of 32