FPGA Package Top View

I/O Bank Usage

<table>
<thead>
<tr>
<th>I/O Bank</th>
<th>Usage</th>
<th>VCCD IO Voltage</th>
<th>VEEP Voltage</th>
<th>VCCIO Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1L</td>
<td>0/0 (--)</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>B1L</td>
<td>0/14 (0 %)</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>C1L</td>
<td>0/14 (0 %)</td>
<td>--</td>
<td>--</td>
<td>--</td>
</tr>
<tr>
<td>D1A</td>
<td>0/16 (16 %)</td>
<td>2.5V</td>
<td>--</td>
<td>2.5V</td>
</tr>
<tr>
<td>E1B</td>
<td>2/31 (21 %)</td>
<td>2.5V</td>
<td>--</td>
<td>2.5V</td>
</tr>
<tr>
<td>F1A</td>
<td>3/48 (48 %)</td>
<td>2.5V</td>
<td>--</td>
<td>2.5V</td>
</tr>
<tr>
<td>G1A</td>
<td>4/7 (7 %)</td>
<td>2.5V</td>
<td>--</td>
<td>2.5V</td>
</tr>
<tr>
<td>H1A</td>
<td>5/10 (10 %)</td>
<td>1.5V</td>
<td>0.75V</td>
<td>2.5V</td>
</tr>
<tr>
<td>I1A</td>
<td>6/15 (15 %)</td>
<td>1.5V</td>
<td>0.75V</td>
<td>2.5V</td>
</tr>
<tr>
<td>J1A</td>
<td>7/23 (18 %)</td>
<td>1.5V</td>
<td>0.75V</td>
<td>2.5V</td>
</tr>
<tr>
<td>K1A</td>
<td>8/27 (27 %)</td>
<td>1.5V</td>
<td>0.75V</td>
<td>2.5V</td>
</tr>
<tr>
<td>L1A</td>
<td>9/37 (10 %)</td>
<td>1.5V</td>
<td>0.75V</td>
<td>2.5V</td>
</tr>
</tbody>
</table>

Top View - Wire Bond

Cyclone V - 5CSXFC5C6U23C7
Cyclone V SoC Transceivers & Clocks

CAD Note: Place resistor near RREF_TL pins. Route away from aggressor.

Title
Size
Document Number
Rev
Date
Sheet

ALTHELIO SOC-R1.4

ALTHIMA Corporation
1-5-5, Shin-Yokohama, Kouhoku-ku, Yokohama, 222-8563 JAPAN

STEP
Cyclone V SoC Configuration

Configuration mode: Active Serial x4
POR Delay: Fast
10/100/1000 Ethernet - HPS

**ETHERNET INTERFACE**

- ENET_HPS_TXD[3..0]
- ENET_HPS_GTX_CLK
- ENET_HPS_TX_EN
- ENET_HPS_MDC
- ENET_HPS_RESETn
- ENET_HPS_RXD[3..0]
- ENET_HPS_RX_CLK
- ENET_HPS_RX_DV
- ENET_HPS_MDIO
- ENET_HPS_INTn

**MDI INTERFACE**

- MDI_HPS_P1
- MDI_HPS_N1
- MDI_HPS_P2
- MDI_HPS_N2
- MDI_HPS_P3
- MDI_HPS_N3

**Boot-Straps**

- 3.3V
- 1.2V_AVDDL_PLL

**I2C Address = 0x51**

- Place near KSZ9021RN PHY

**Note:**

- Dedicated reset Consider to connect expander and pull down

**Designed by:**

- ALTHELIO SOIC-R1.4

**ALTIMA Corporation**

1-5-5, Shin-Yokohama, Kouhoku-ku, Yokohama, 222-8563 JAPAN

**Date:**

- NOV. 20, 2013
QSPI Flash & Reset Circuit

Not Mount

PLACE NEAR QSPI FLASH
UART

3.3V_USB is CP2103 supply voltage.
Power Monitor

**I2C Address = 0x5C**
Power 1 - DC Input, 1.1V
Power 2 - 3.3V

Regulator input caps
Place near regulator controller
Power3 - 1.5V, DDR3 VREF & VTT

- Cad Note: Regulator input caps Place near regulator controller
- Cad Note: Power2 output caps Place near inductor
- Design Note: Prefer 0603 size caps
- 25V rated voltage is sufficient

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- Cad Note: Place output caps near inductor
- Cad Note: Place regulator input caps near regulator controller
- Design Note: Prefer 0603 size caps
- 25V rated voltage is sufficient
Design Note: Prefer 0603 size cap. 25V rated voltage is sufficient.

牡 Note: Place output caps near inductor.

Cad Note: Regulator input caps. Place near regulator controller.

Power4 - 2.5V, 5V, 1.8V
Design Note: Prefer 0603 size caps. 25V rated voltage is sufficient.

Cad Note: Place output caps near inductor.

Cad Note: Regulator input caps. Place near regulator controller.