Description

• The Block diagram consists of a TV IN interface which takes NTSC/PAL composite input. The BT656 video format is converted to Avalon Streaming interface by passing through Altera Clocked Video input IP. The YCbCr color space of the input is then changed to RGB format using Altera VIP cores and given as one of the input to the Alpha blending mixer. The FPGA DDR3 memory is used to buffer the input video stream.

• The implementation also consists of a 32bit frame reader for reading the QT graphics data or the Linux OS image dumped in HPS DDR3 memory. This image consists of 24bit RGB data and 8bit alpha value for varying the transparency of the layer. This image will be overlaid on the input streaming video.

• The two layers are alpha blended and displayed on an LCD monitor of 800x480 resolution.

• The Altera VIP cores are connected to HPS via the HPS to FPGA AXI lightweight bridge and can be controlled during run time.