



NovTech Platform Evaluation Kit

NOVPEK™CVLite

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Revision History

| Revision Number | Date | Changes | Notes |
|-----------------|---------|-----------------|-------|
| 1.0 | 10/2014 | Initial Release | |

Table 1 - Provides a revision history for this document.

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1. Introduction

This document describes the NOVPEK™CVLite Development Board. This Reference Manual assists the user with setup and configuration of the development board's jumpers and switches. Users will be able to familiarize themselves with the board and its peripherals to begin testing, evaluating and developing with the Altera® Cyclone™ V SoC FPGA. The board contains peripherals such as 1G Ethernet (PHY & connector), USB OTG (PHY & connector), UART to USB (IC & Connector), SD card slot, JTAG, and FPGA PIN Headers. The NOVPEK™CVLite provides a quick solution for evaluating and prototyping any project considering the use of the Altera® Cyclone™ V SoC.

1.1 NOVPEK™CVLite

The NOVPEK™CVLite contains all necessary components needed to use the board. A Linux based Virtual Machine is also provided with all the necessary software tools needed to evaluate, modify, and develop for the board.

1.2 Package Contents



Figure 1- NOVPEK™CVLite Development Kit

Included in the NOVPEK™CVLite

- The NOVPEK™CVLite Base Board
- The NOVSOM™CVLite Module (installed)
- 4G SD card with bootable Linux (inserted)
- 5V Power Supply
- Quick Start Guide
- USB Cable (Type B) for UART
- Ethernet Cable
- 16G USB Drive

1.3 Getting Help

For further help and support please contact your local Arrow FAE.

2. Board Components

This section describes the NOVPEK™CVLite and its components.

Below is a picture of the board and a description of its components, and connectors.

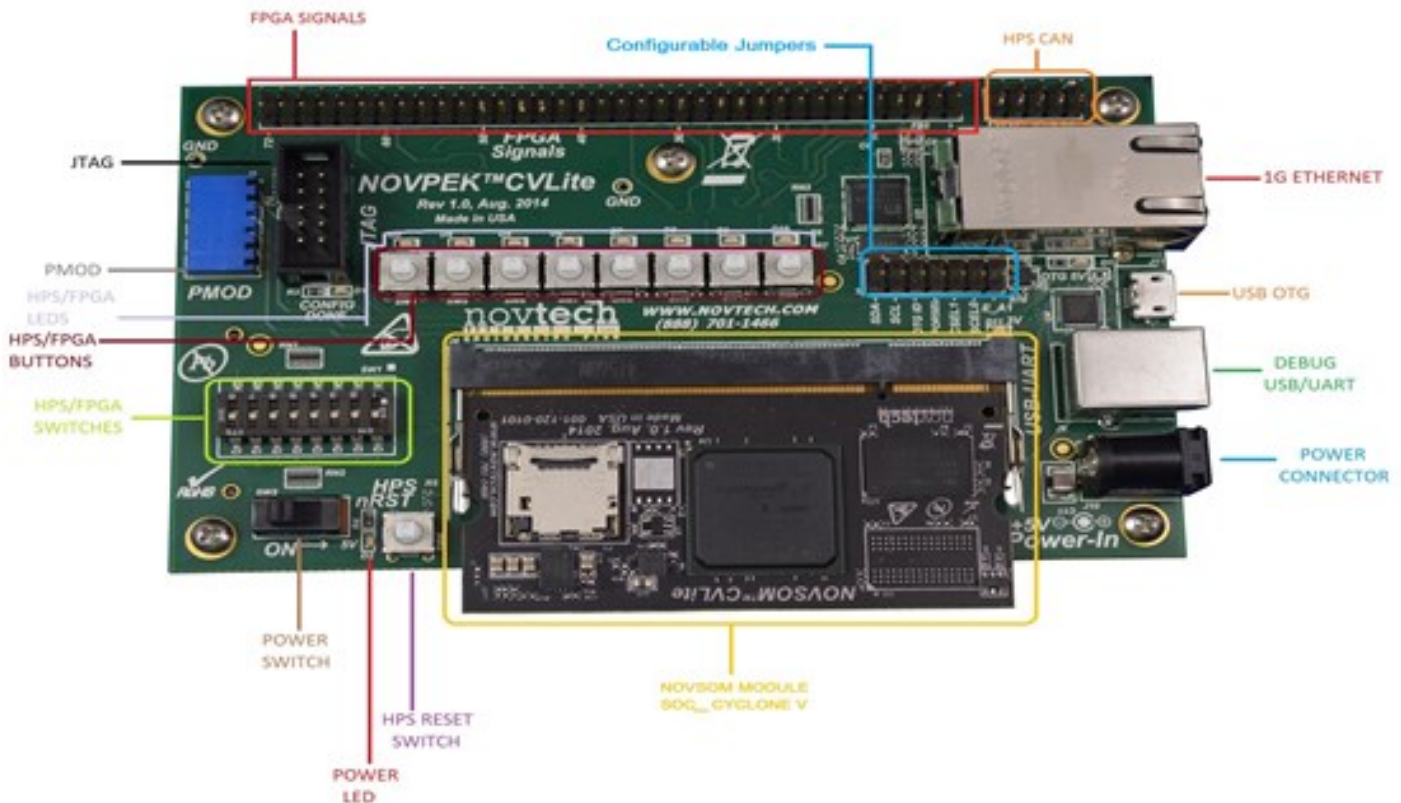


Figure 2 - NOVPEK™CVLite Board

2.1 SoC Module (NOVSOM™CVLite)

- Cyclone™ V SoC (U19 package).
- Single/Dual Core ARM® Cortex™ A9.
- Up to 1GByte DDR3.
- HPS boot from SD (optional SPI-NOR boot).
- HPS configures the FPGA (optional SPI-NOR configuration device).
- On module power solution, requires a 5V power in.
- On board 2K EEPROM with built-in MAC address.

2.2 Debug

- USB Blaster header.

2.3 Bootable Memory Device

- SD Card Socket (in parallel with Micro SD on the SoM).

2.4 Communication Devices

- USB to UART (Debug UART).
- USBOTG 2.0 (HPS).
- CAN (HPS).
- 10/100/1000 Ethernet (HPS).
- PMOD with support for UART/I2C, SPI (FPGA).

2.5 Connectors

- HPS/FPGA JTAG.
- HPS CSEL/PORSEL Pin Header.
- FPGA PIN Headers.

2.6 Switches, Buttons and LEDs

- 8 User Keys (FPGA x 4, HPS x 4).
- 7 User Switches (FPGA x 3, HPS x 4).
- 8 User LEDs (FPGA x 4, HPS x 4).
- HPS Warm Reset Button.
- USBOTG LED.
- Power Switch.
- 5V Power Status LED.
- 3.3V Power Status LED.
- DS-5/SignalTap USB Blaster selector.

2.7 Power

- 5V DC input.

2.8 Block Diagram

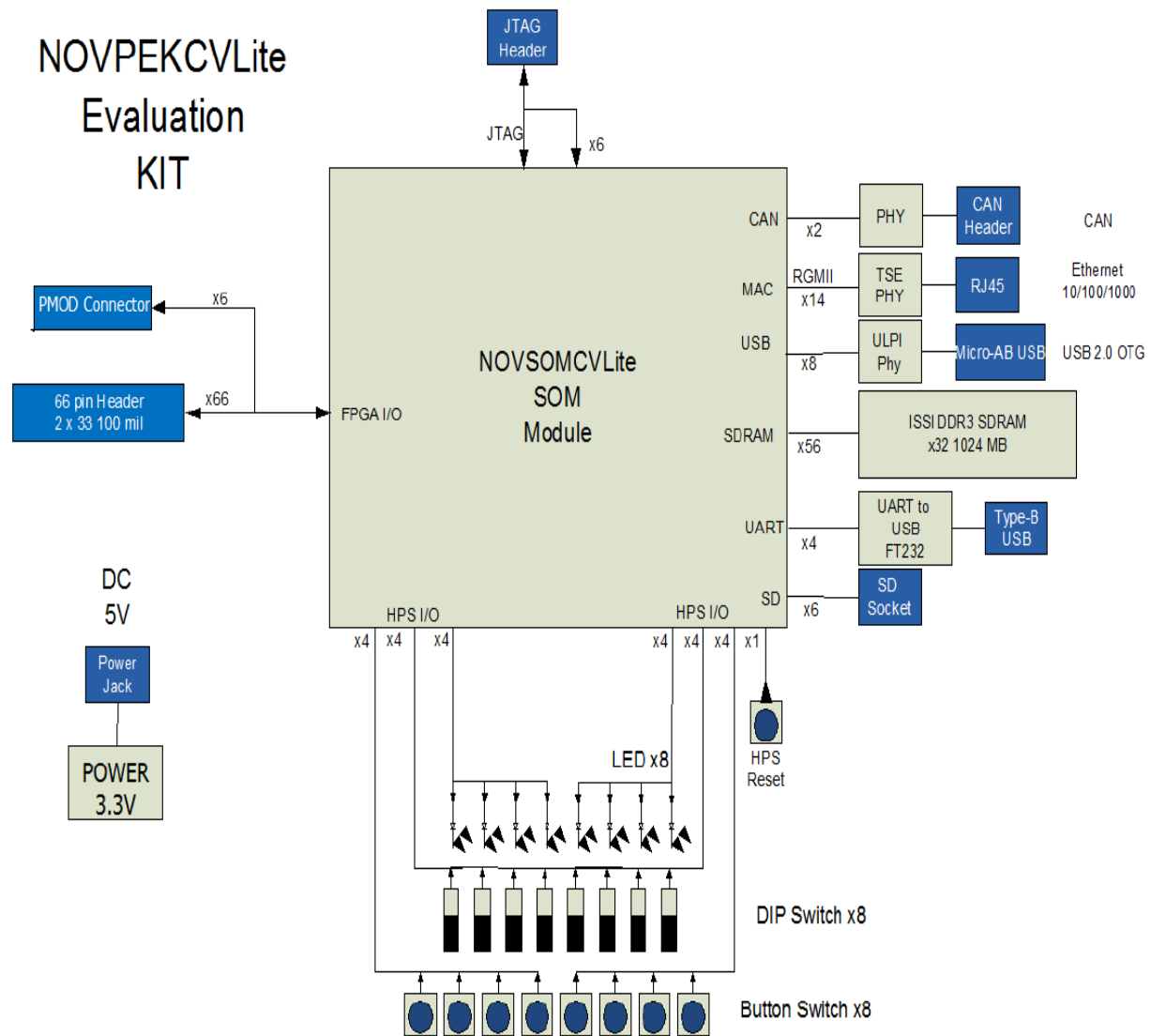


Figure 3 - Block Diagram

3. Setup the Development Board

3.1 Dip-Switch Configuration Options

Dip-Switch SW1-8 must be in the 'OFF' position in order for the board to boot. After boot it can be used as an input to the HPS GPIO.

Dip-Switch SW1-4 selects between using the USB Blaster in DS-5 ('ON' position) or SignalTap ('OFF' position') mode. The other 6 Dip-Switches are for general use.

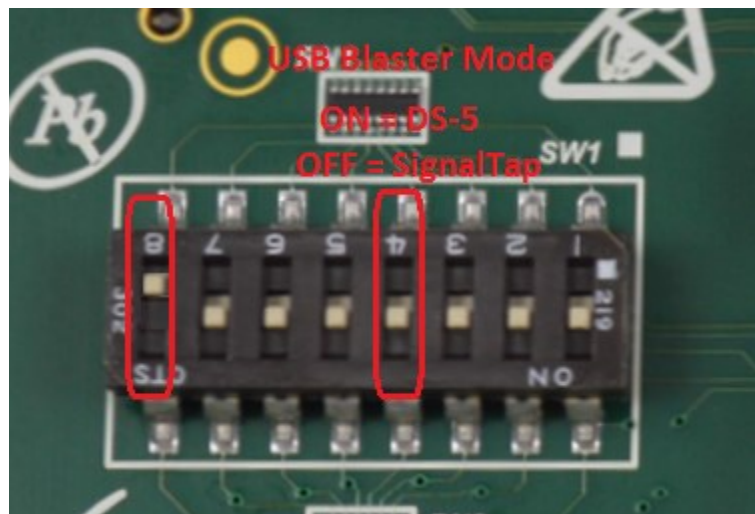


Figure 4 – Board Dip-Switch Configuration

3.2 Configuration Jumpers

The NOVPEK™CVLite has a number of jumpers (J6) that can be used to configure the NOVOSOM™CVL Module. Please see Figure 5 and Table 2 below for details.



Figure 5 – Configuration Connector

Table 2-Configuration Connector pin out

| Pin Name | Signal | Jumper Open | Jumper Close |
|----------|----------------------|----------------------------------|---------------------------------------|
| SDA | VCCIO7A_HPS_I2C0_SDA | | Connected to MAC EEPROM SDA |
| SCL | VCCIO7A_HPS_I2C0_SCL | | Connected to MAC EEPROM SCL |
| OTG ID | USBOTG_HPS_ID | Signal is Floating | Connected to GND, Force Host Mode |
| PORSEL | VCCRSTCLK_HPS_PORSEL | Signal is pull-up by the NOVOSOM | Connected to GND, PORSEL set to LOW |
| CSEL1 | VCCIO7A_HPS_UART0_TX | Signal is pull-up by the NOVOSOM | Signal is pull-low, PORSEL set to LOW |
| SCELO | VCCIO7A_HPS_CAN0_TX | Signal is pull-up by the NOVOSOM | Signal is pull-low, PORSEL set to LOW |
| E_A1 | NOVSOM_MAC_EEPROM_A1 | Signal is pull-up by the NOVOSOM | EEPROM I2C address is 0xA0/0xA1 |

3.3 JTAG Connector

The NOVPEK™CVLite has a JTAG connector for debugging the NOVOSOM™CVL Module. This can be used for FPGA image downloads, SignalTap ELA and ARM®DS-5 debug sessions.

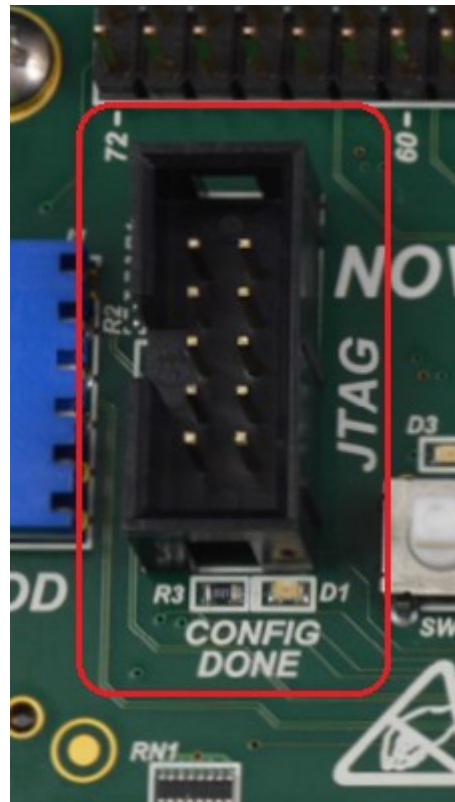


Figure 6 – JTAG Header

3.4 Board LED's

The NOVPEK™CVLite includes the following LEDs:

- D2 - 5V indicator (Power In)
- D11 - 3.3V indicator (generated by NOVOSOM™CVLite)
- D1 - Cyclone™ V FPGA CONFIG_DONE
- D3, D4, D5, D6 - Driven by HPS GPIO
- D7, D8, D9 & D10 - Driven by FPGA GPIO

3.5 Board Power Switch

The board power switch (SW2) connects 5V from the power supply to the base board and the module.

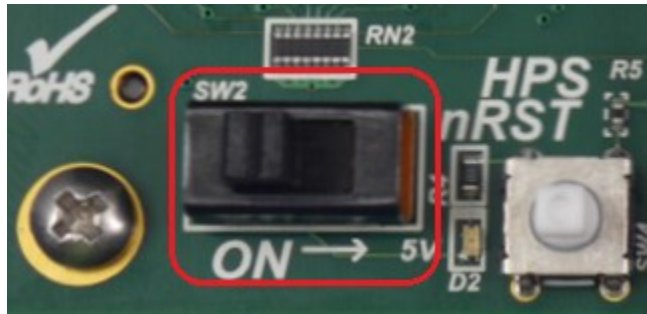


Figure 7F - Board Power Switch

3.6 Board Reset Switch

The board has a reset button (SW4) connected to the HPS nRST (warm reset).

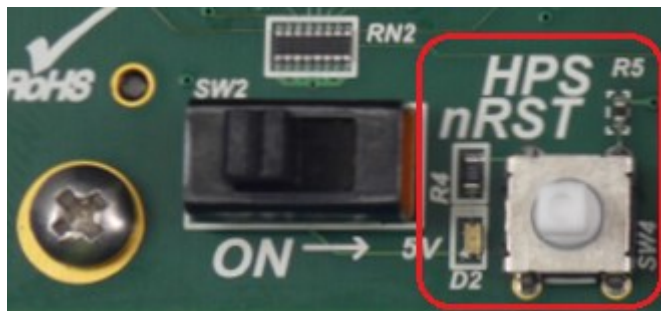


Figure 8 - Board Reset Buttons

4 FPGA Interface

This section describes the different interfaces connected to the FPGA on the NOVPEK™CVLite. Interfaces such as Switches, LEDs, and Push Buttons can all be driven by FPGA logic.

4.1 FPGA Push Buttons

The NOVPEK™CVLite provides four push-button switches (SW8, SW9, SW10, and SW11) for FPGA use. Each push-button switch provides a high logic level when it is not pressed, and provides a low logic level when depressed.



Figure 9 - FPGA Push Button

Table 3 - FPGA Push Button pin assignments

| Button | Designator | SIGNAL | BGA Ball | FPGA PIO | Note |
|----------|------------|------------------------|----------|---------------|-----------------------|
| FPGA_PB0 | SW11 | VCCIO7A_HPS_SPIM0_SS0 | D14 | BUTTON_PIO[0] | HPS Loaner IO to FPGA |
| FPGA_PB1 | SW10 | VCCIO7A_HPS_SPIM0_MISO | A20 | BUTTON_PIO[1] | HPS Loaner IO to FPGA |
| FPGA_PB2 | SW9 | VCCIO7A_HPS_TRACE_CLK | B15 | BUTTON_PIO[2] | HPS Loaner IO to FPGA |
| FPGA_PB3 | SW8 | VCCIO7A_HPS_TRACE_D0 | D19 | BUTTON_PIO[3] | HPS Loaner IO to FPGA |

4.2 FPGA Dip-Switches

The NOVPEK™CVLite provides three dip-switches(SW1-1, SW1-2 and SW1-3) for FPGA use. When the switch is in the 'ON' position (closest to the edge of the board), it provides a low logic level. When the switch is in the 'OFF' position it provides a high logic level.

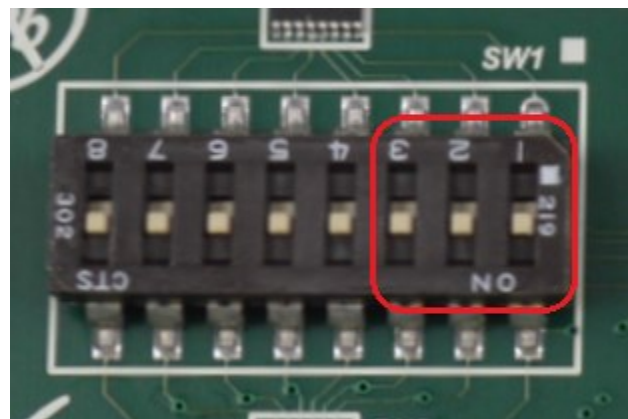


Figure 10 - FPGA Dip-Switches

Table 4 - FPGA Dip-Switches pin assignments

| DIP SW | Designator | SIGNAL | BGA Ball | FPGA PIO | Note |
|-------------|------------|---------------------------|----------|--------------|-----------------------|
| FPGA_DIPSW0 | SW1-1 | VCCIO7C_HPS_SDMMC_CLK_IN | C10 | DIPSW_PIO[0] | HPS Loaner IO to FPGA |
| FPGA_DIPSW1 | SW1-2 | VCCIO7C_HPS_SDMMC_PWREN | E8 | DIPSW_PIO[1] | HPS Loaner IO to FPGA |
| FPGA_DIPSW2 | SW1-3 | VCCIO7D_HPS_RGMII0_TX_CLK | H7 | DIPSW_PIO[2] | HPS Loaner IO to FPGA |

4.3 FPGA LED's

The NOVPEK™CVLite provides four LED's (D7, D8, D9 & D10) for FPGA use. Driving its associated pin to a high logic level turns the LED on, driving the pin low turns it off.

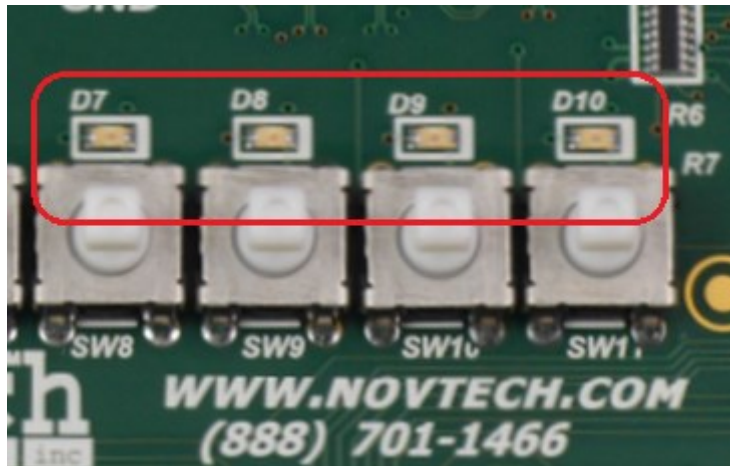


Figure 11 - FPGA LED's

Table 5 - FPGA LED's pin assignments

| LED | Designator | SIGNAL | BGA Ball | FPGA PIO | Note |
|-----------|------------|------------------------|----------|------------|-----------------------|
| FPGA_LED0 | D10 | VCCIO7A_HPS_SPIMO_MOSI | A22 | LED_PIO[0] | HPS Loaner IO to FPGA |
| FPGA_LED1 | D9 | VCCIO7A_HPS_SPIMO_CLK | A21 | LED_PIO[1] | HPS Loaner IO to FPGA |
| FPGA_LED2 | D8 | VCCIO7A_HPS_TRACE_D1 | C15 | LED_PIO[2] | HPS Loaner IO to FPGA |
| FPGA_LED3 | D7 | VCCIO7A_HPS_TRACE_D2 | C20 | LED_PIO[3] | HPS Loaner IO to FPGA |

4.4 FPGA I/O

There are 66¹ user-controllable IO's connected to the SoC FPGA on the NOVPEK[™]CVLite. Each LVDS pair is routed differentially on the NOV SOM[™]CVLite and the NOVPEK[™]CVL base board.

Table 6 - J2 odd pin assignments

| Pin Number | SIGNAL | BGA Ball | Note |
|------------|----------------------------|----------|-----------------------|
| 1 | VCCIO8A_DIFFIO_TX_T4_P | A6 | Differentially routed |
| 3 | VCCIO8A_DIFFIO_TX_T4_N | A5 | Differentially routed |
| 5 | VCCIO5A_DIFFIO_TX_R5_N | AA22 | Differentially routed |
| 7 | VCCIO5A_DIFFIO_TX_R5_P | AB22 | Differentially routed |
| 9 | VCCIO5A_DIFFIO_TX_R3_N | Y21 | Differentially routed |
| 11 | VCCIO5A_DIFFIO_TX_R3_P | AA21 | Differentially routed |
| 13 | VCCIO5A_DIFFIO_TX_R1_N | Y20 | Differentially routed |
| 15 | VCCIO5A_DIFFIO_TX_R1_P | Y19 | Differentially routed |
| 17 | VCCIO5A_DIFFIO_RX_R2_N | W18 | Differentially routed |
| 19 | VCCIO5A_DIFFIO_RX_R2_P | V17 | Differentially routed |
| 21 | VCCIO4A_DIFFIO_TX_B45_N | AB17 | Differentially routed |
| 23 | VCCIO4A_DIFFIO_TX_B45_P | AA16 | Differentially routed |
| 25 | VCCIO4A_DIFFIO_RX_B47_N | Y14 | Differentially routed |
| 27 | VCCIO4A_DIFFIO_RX_B47_P | W14 | Differentially routed |
| 29 | VCCIO4A_DIFFIO_TX_B48_N | AB20 | Differentially routed |
| 31 | VCCIO4A_DIFFIO_TX_B48_P | AB19 | Differentially routed |
| 33 | VCCIO4A_DIFFIO_RX_B43_N | W11 | Differentially routed |
| 35 | VCCIO4A_DIFFIO_RX_B43_P | V11 | Differentially routed |
| 37 | VCCIO4A_DIFFIO_TX_B41_P | Y11 | Differentially routed |
| 39 | VCCIO4A_DIFFIO_TX_B41_N | AA11 | Differentially routed |
| 41 | VCCIO4A_DIFFIO_RX_B46_N | AB15 | Differentially routed |
| 43 | VCCIO4A_DIFFIO_RX_B46_P | AA15 | Differentially routed |
| 45 | VCCIO3B_DIFFIO_TX_B37_N | AB10 | Differentially routed |
| 47 | VCCIO3B_DIFFIO_TX_B37_P | AB9 | Differentially routed |
| 49 | VCCIO3A_DIFFIO_TX_B8_N | W8 | Differentially routed |
| 51 | VCCIO3A_DIFFIO_TX_B8_P | V9 | Differentially routed |
| 53 | VCCIO3A_DIFFIO_RX_B3_N | U6 | Differentially routed |
| 55 | VCCIO3A_DIFFIO_RX_B3_N | V6 | Differentially routed |
| 57 | VCCIO3A_DIFFIO_RX_B1_P | W6 | Differentially routed |
| 59 | VCCIO3A_DIFFIO_RX_B1_N | Y5 | Differentially routed |
| 61 | VCCIO3A_DIFFIO_TX_B2_N | AB5 | Differentially routed |
| 63 | VCCIO3A_DIFFIO_TX_B2_P | AA5 | Differentially routed |
| 65 | <u>FPGA_VCCPGM_nSTATUS</u> | | |
| 67 | <u>FPGA_VCCPGM_nCONFIG</u> | | |
| 69 | VCCIO7A_HPS_CLK2 | | |
| 71 | GND | | |

¹ Please note that a jumper wire on the bottom side on the boards provides a 24MHz clock (from the USBOTG Oscillator) to pin 2 of J2, see board release note for more info

Table 7- J2 even pin assignments

| Pin Number | SIGNAL | BGA Ball | Note |
|------------|-------------------------|----------|-----------------------|
| 2 | VCCIO8A_DIFFIO_RX_T9_P | C6 | Differentially routed |
| 4 | VCCIO8A_DIFFIO_RX_T9_N | C5 | Differentially routed |
| 6 | VCCIO8A_DIFFIO_RX_T1_N | E5 | Differentially routed |
| 8 | VCCIO8A_DIFFIO_RX_T1_P | F5 | Differentially routed |
| 10 | VCCIO5A_DIFFIO_TX_R7_N | W21 | Differentially routed |
| 12 | VCCIO5A_DIFFIO_TX_R7_P | V20 | Differentially routed |
| 14 | VCCIO5A_DIFFIO_RX_R4_N | V19 | Differentially routed |
| 16 | VCCIO5A_DIFFIO_RX_R4_P | U18 | Differentially routed |
| 18 | VCCIO5A_DIFFIO_RX_R6_N | U17 | Differentially routed |
| 20 | VCCIO5A_DIFFIO_RX_R6_P | V16 | Differentially routed |
| 22 | VCCIO5A_DIFFIO_RX_R8_N | W16 | Differentially routed |
| 24 | VCCIO5A_DIFFIO_RX_R8_P | V15 | Differentially routed |
| 26 | VCCIO4A_DIFFIO_RX_B70_N | Y16 | Differentially routed |
| 28 | VCCIO4A_DIFFIO_RX_B70_P | Y15 | Differentially routed |
| 30 | VCCIO4A_DIFFIO_RX_B55_N | Y13 | Differentially routed |
| 32 | VCCIO4A_DIFFIO_RX_B55_P | W12 | Differentially routed |
| 34 | VCCIO4A_DIFFIO_TX_B69_P | AA18 | Differentially routed |
| 36 | VCCIO4A_DIFFIO_TX_B69_N | AB18 | Differentially routed |
| 38 | VCCIO4A_DIFFIO_RX_B42_P | AB12 | Differentially routed |
| 40 | VCCIO4A_DIFFIO_RX_B42_N | AB13 | Differentially routed |
| 42 | VCCIO4A_DIFFIO_TX_B44_P | AA13 | Differentially routed |
| 44 | VCCIO4A_DIFFIO_TX_B44_N | AB14 | Differentially routed |
| 46 | VCCIO3B_DIFFIO_RX_B31_N | V10 | Differentially routed |
| 48 | VCCIO3B_DIFFIO_RX_B31_P | U10 | Differentially routed |
| 50 | VCCIO3B_DIFFIO_RX_B39_N | AB8 | Differentially routed |
| 52 | VCCIO3B_DIFFIO_RX_B39_P | AA8 | Differentially routed |
| 54 | VCCIO3A_DIFFIO_RX_B5_N | V7 | Differentially routed |
| 56 | VCCIO3A_DIFFIO_RX_B5_P | U7 | Differentially routed |
| 58 | VCCIO3A_DIFFIO_RX_B7_P | V6 | Differentially routed |
| 60 | VCCIO3A_DIFFIO_RX_B7_N | W7 | Differentially routed |
| 62 | VCCIO3A_DIFFIO_TX_B6_P | Y8 | Differentially routed |
| 64 | VCCIO3A_DIFFIO_TX_B6_N | AA7 | Differentially routed |
| 66 | VCCIO3A_DIFFIO_TX_B4_P | AA6 | Differentially routed |
| 68 | VCCIO3A_DIFFIO_TX_B4_N | AB7 | Differentially routed |
| 70 | +3.3V | | |
| 72 | +5.0V | | |

4.5 PMOD™ Connector

PMOD™ is a standard defined by DIGILENT® (www.digilent.com). This standard make use of I2C/UART/SPI/GPIO interfaces to communicate with an array of available modules. The NOVPEK™CVLite has a 6 pin header to support PMOD™ (J1), two power pins and four signals. Logic in the FPGA can be used to drive any of the communication interfaces of the PMOD™.

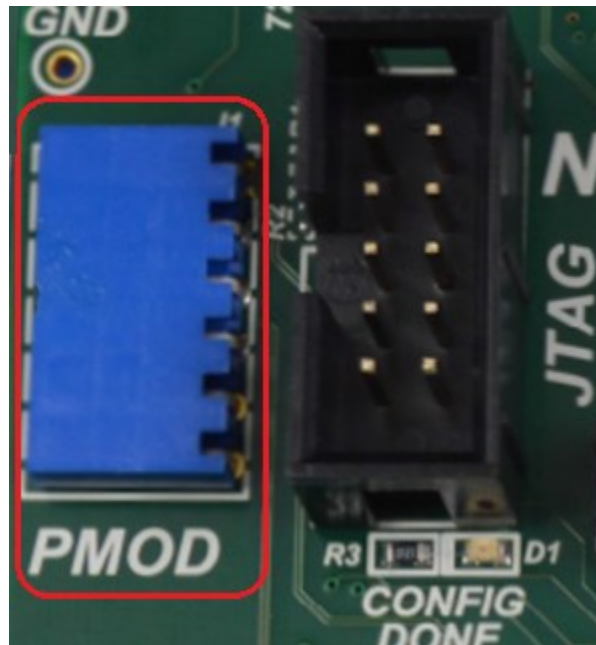


Figure 12 – PMOD™ Connector

Table 8 – PMOD™ (J1) pin assignments

| PMODE Pin | SIGNAL | BGA Ball | Note |
|-----------|------------------------|----------|-----------------------|
| 1 | VCCIO3A_DIFFIO_TX_B6_P | Y8 | Shared with J2 pin 62 |
| 2 | VCCIO3A_DIFFIO_TX_B6_N | AA7 | Shared with J2 pin 64 |
| 3 | VCCIO3A_DIFFIO_TX_B4_P | AA6 | Shared with J2 pin 66 |
| 4 | VCCIO3A_DIFFIO_TX_B4_N | AB7 | Shared with J2 pin 68 |
| 5 | GND | | |
| 6 | +3.3V | | |

5 HPS Interface

This section describes the different interfaces connected to the HPS on the NOVPEK™CVLite.

5.1 HPS Push Buttons

The NOVPEK™CVLite provides four push-button switches (SW3, SW5, SW6, and SW7) for HPS use. Each push-button switch provides a high logic level when it is not pressed, and provides a low logic level when depressed.

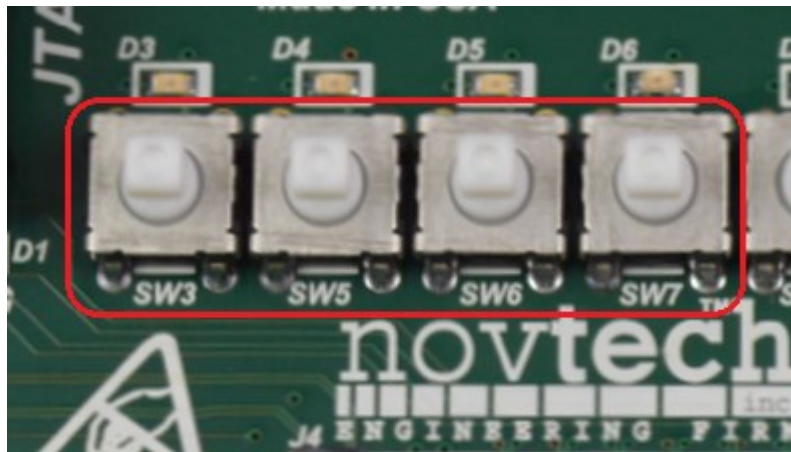


Figure 13 – HPS Push Buttons

Table 9 – HPS Push Button pin assignments

| Button | Designator | SIGNAL | BGA Ball | HPS GPIO | Note |
|---------|------------|----------------------|----------|-----------|------|
| HPS_PB0 | SW7 | VCCIO7A_HPS_TRACE_D3 | F13 | GPIO1[23] | |
| HPS_PB1 | SW6 | VCCIO7A_HPS_TRACE_D5 | C14 | GPIO1[25] | |
| HPS_PB2 | SW5 | VCCIO7B_HPS_QSPI_CLK | C11 | GPIO1[0] | |
| HPS_PB3 | SW3 | VCCIO7B_HPS_QSPI_IO0 | D11 | GPIO1[5] | |

5.2 HPS Dip-Switches

The NOVPEK™CVLite provides four dip-switches (SW1-5, SW1-6, SW1-7 and SW1-8) for HPS use. When the switch is in the 'ON' position (closer to the edge of the board), it provides a low logic level. When the switch is in the 'OFF' position it provides a high logic level.

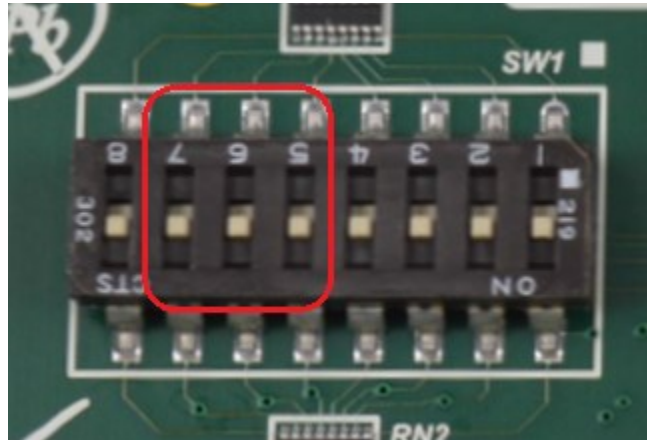


Figure 14 - HPS Dip-Switches

Table 10 - HPS Dip-Switches Pin Assignments

| DIP SW | Designator | SIGNAL | BGA Ball | HPS GPIO | Note |
|------------|------------|----------------------|----------|-----------|-------------------------------------|
| HPS_DIPSW0 | SW1-5 | VCCIO7B_HPS_QSPI_IO1 | D12 | GPPIO1[1] | Must set to 'OFF' to allow HPS boot |
| HPS_DIPSW1 | SW1-6 | VCCIO7B_HPS_QSPI_IO2 | F10 | GPIO1[2] | |
| HPS_DIPSW2 | SW1-7 | VCCIO7B_HPS_QSPI_IO3 | F11 | GPIO1[3] | |
| HPS_DIPSW3 | SW1-8 | VCCIO7B_HPS_NAND_WE | B12 | GPIO1[28] | |

5.3 HPS LED's

The NOVPEK[™]CVLite provides four LED's (D3, D4, D5 & D6) for HPS use. Driving its associated pin to a high logic level turns the LED on, driving the pin low turns it off.

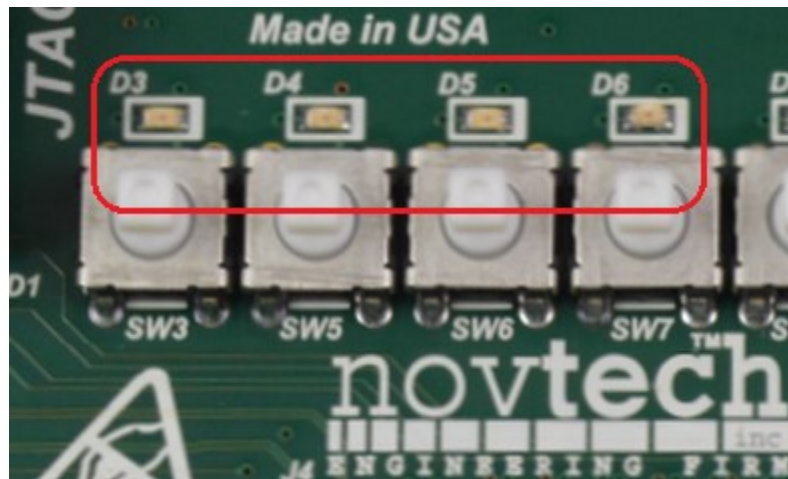


Figure 15 - HPS LED's

Table 11 – HPS LED's pin assignments

| LED | Designator | SIGNAL | BGA Ball | HPS GPIO | Note |
|----------|------------|----------------------|----------|-----------|------|
| HPS_LED0 | D6 | VCCIO7A_HPS_TRACE_D4 | C19 | GPIO1[24] | |
| HPS_LED1 | D5 | VCCIO7A_HPS_TRACE_D6 | B19 | GPIO1[26] | |
| HPS_LED2 | D4 | VCCIO7A_HPS_TRACE_D7 | B20 | GPIO1[27] | |
| HPS_LED3 | D3 | VCCIO7B_HPS_QSPI_SS0 | A11 | GPIO1[4] | |

5.4 HPS Ethernet

The SoC FPGA HPS Ethernet MAC connects to a Micrel KSZ9031RN PHY via an RGMII interface. Please refer to the NOVPEK™CVLite schematic for connection details.

5.5 HPS Terminal UART

The board has one UART interface connected for communication with the HPS. This interface does not support HW flow control signals. The physical interface is done using UART-USB onboard bridge based on FT232RQ chip and connects to the host using a USB Type B connector (J9). The FT232RQ is powered by the USB cable, so the UART interface can be active immediately upon the board boot. Please verify that the port is connected to the PC and a terminal software is running on the PC (115200 Baud, 8 bit, 1 stop, no hardware flow control) before applying power to the board. Please refer to the NOVPEK™CVLite schematic for connection details.

5.6 HPS SD Slot

The SD slot (P1) on the base board as the same signals connection as the \square SD on the NOV SOM™CVLite, it provides an eraser mechanical access to the SD during software development. Make sure that only one of the slots is occupied with a card, if both are occupied the boot will be halt. Please refer to the NOVPEK™CVLite schematic for connection details.

5.7 HPS USBOTG

The NOVPEK™CVLite provides USB interfaces using MICROCHIP USB3300 USBOTG PHY with a microUSB AB type connector (J11). The PHY can operate in Host or Device modes. When operating in Host mode the interface will supply power to the device through a 500mA power limit switch (U3). Please refer to the NOVPEK™CVLite schematic for connection details.

5.8 HPS CAN Bus

The NOVPEK™CVLite provides a CAN interface using TI SN65HVD230 transceiver. The transceiver is designed to provide differential transmit capability to the bus and differential receive capability to a CAN controller on the HPS to a speed of up to 1Mbps. Please refer to the NOVPEK™CVLite schematic for connection details.