

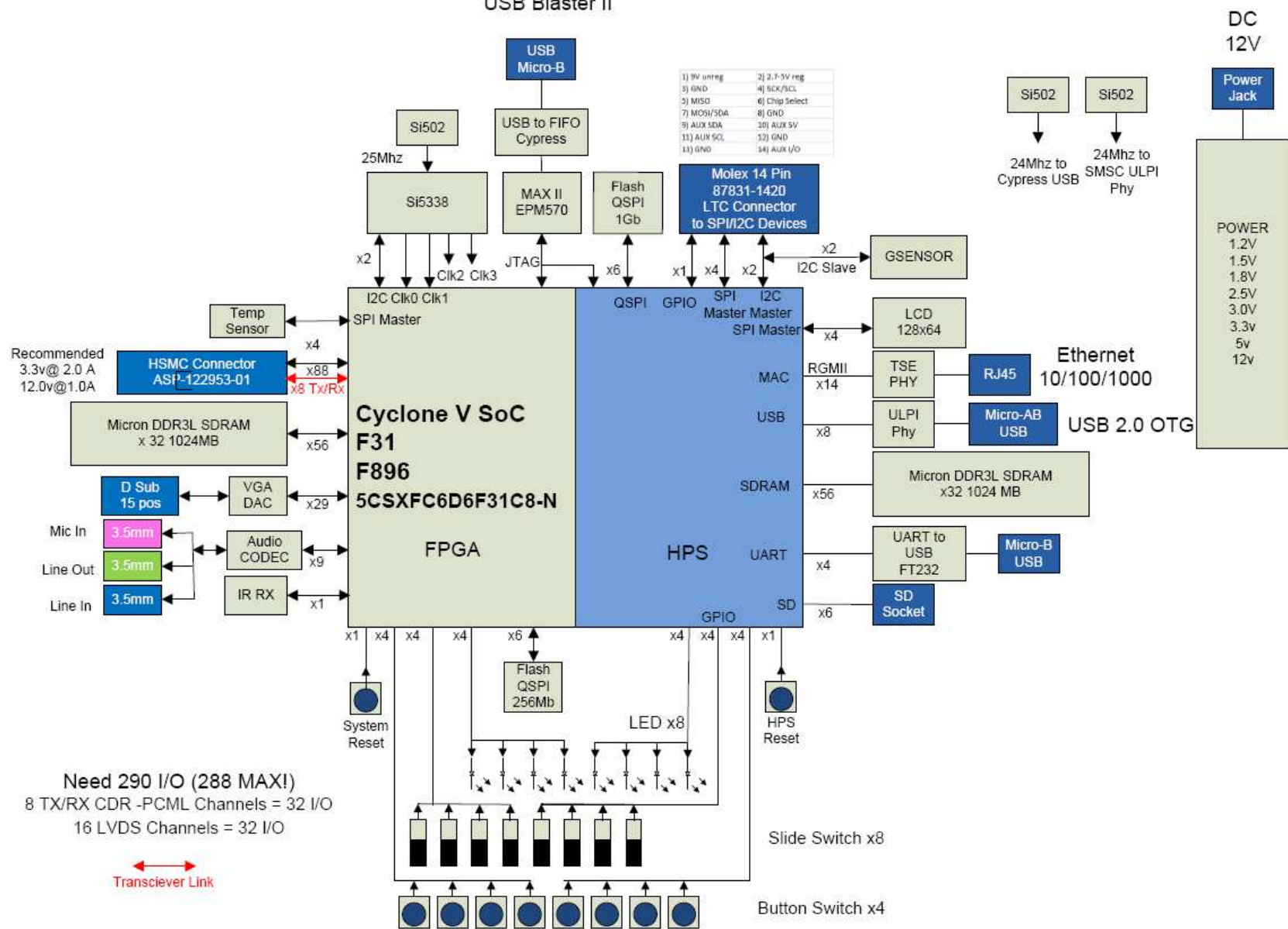
C5S

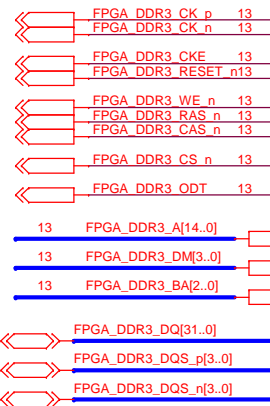
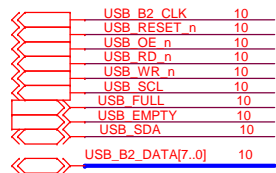
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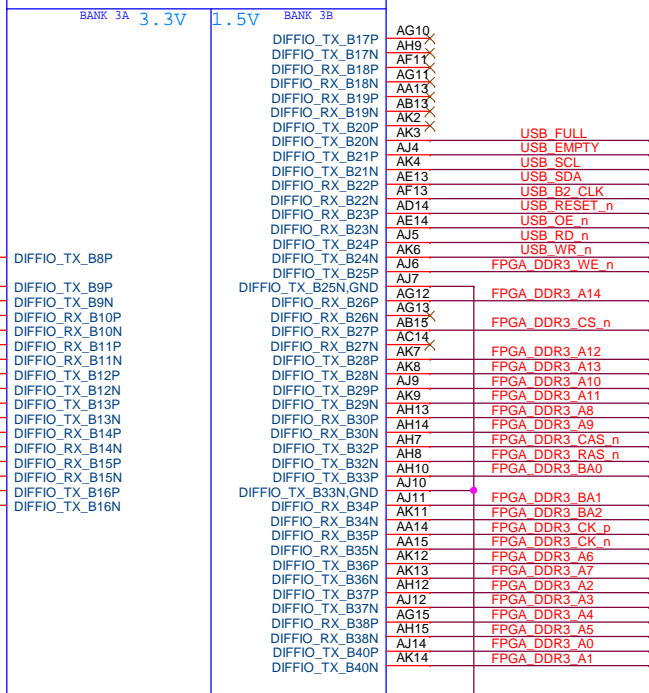
USB Blaster II





U25C

BANK 3

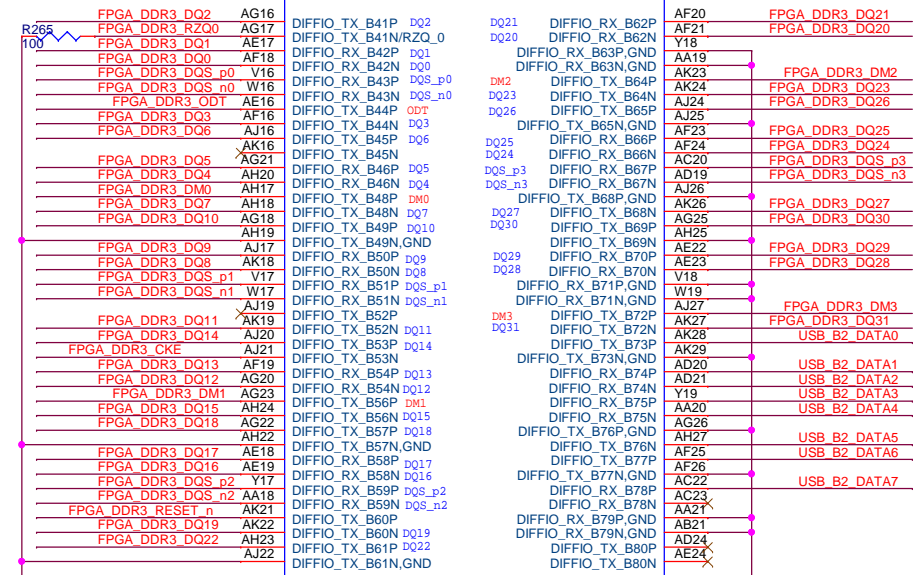


5CSXF6DF31

GND

U25D

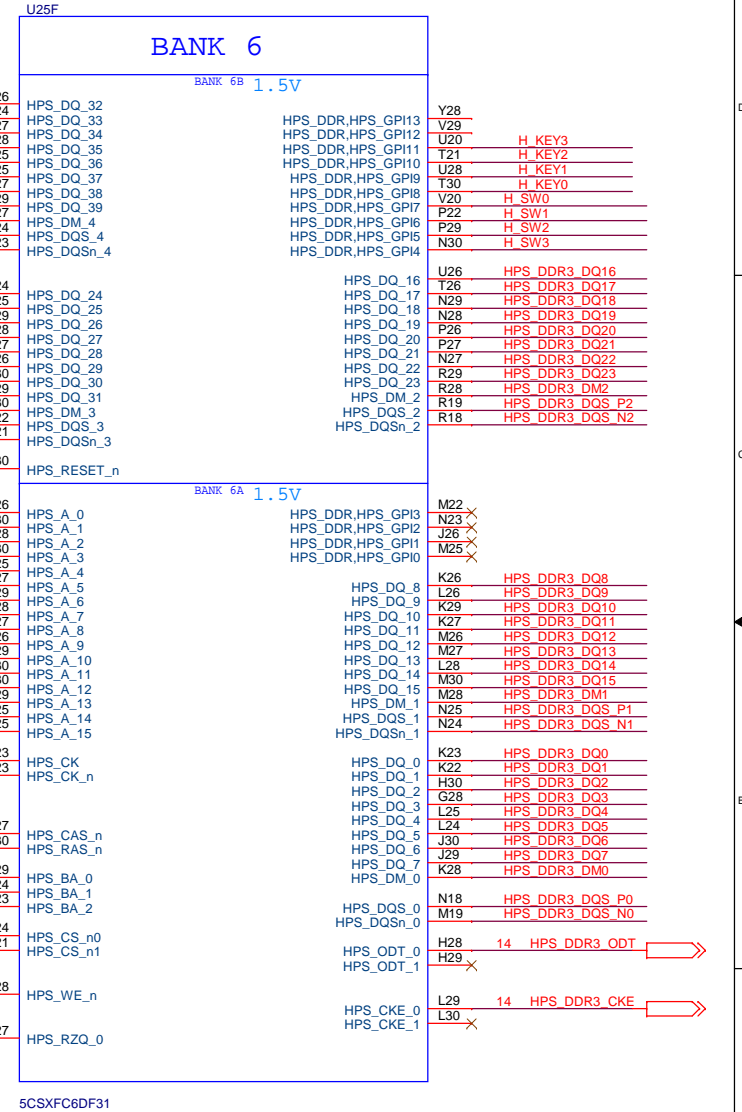
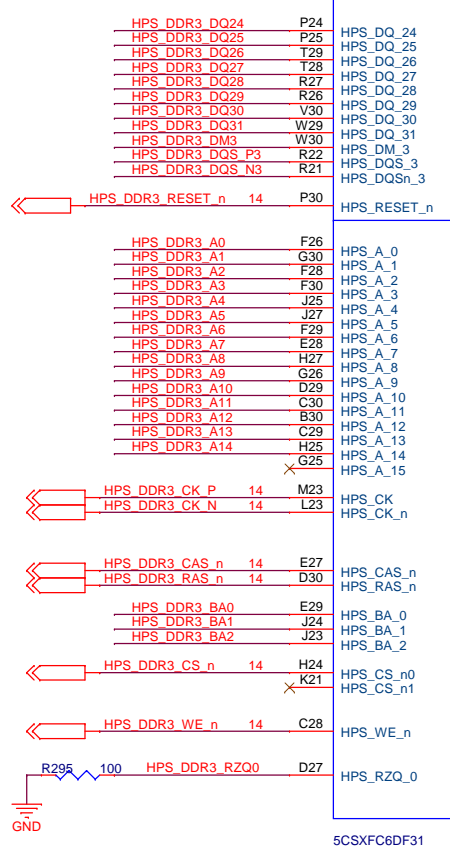
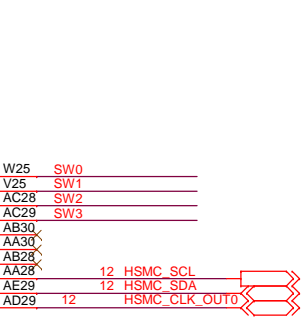
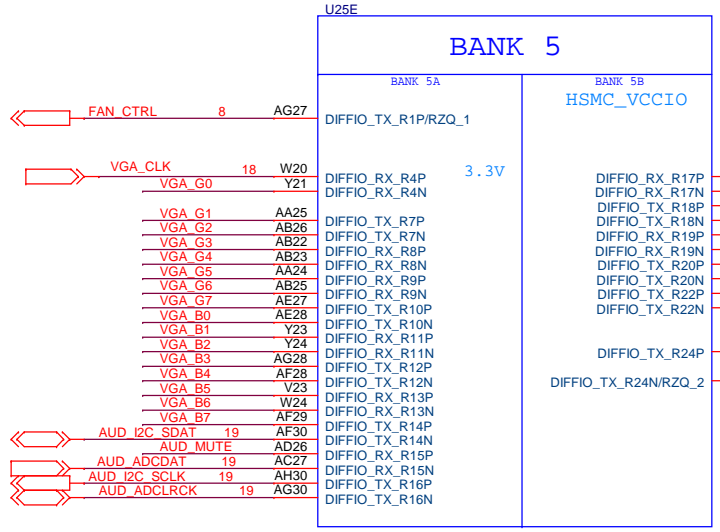
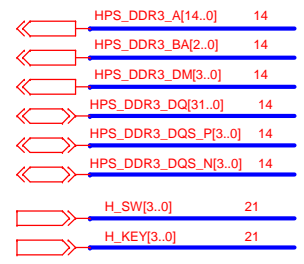
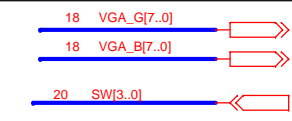
BANK 4A 1.5V

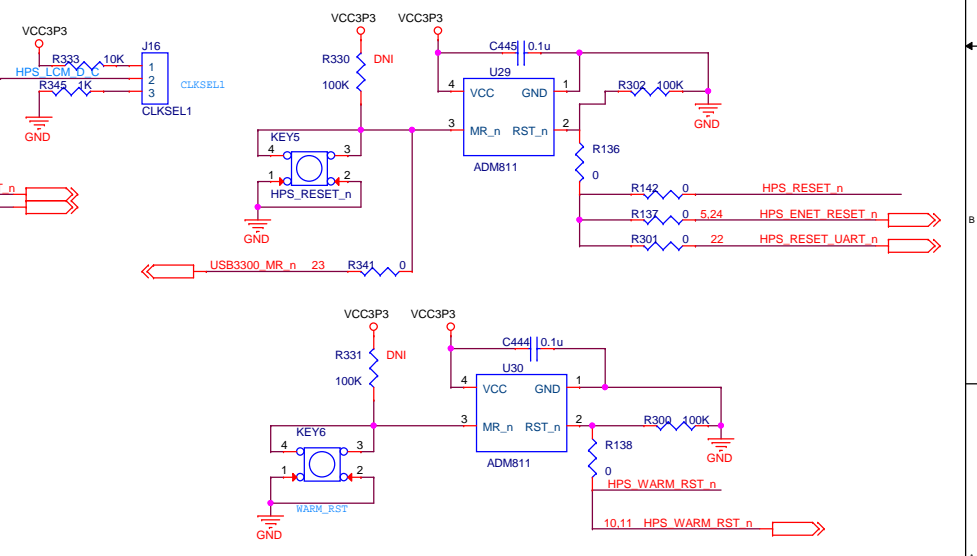
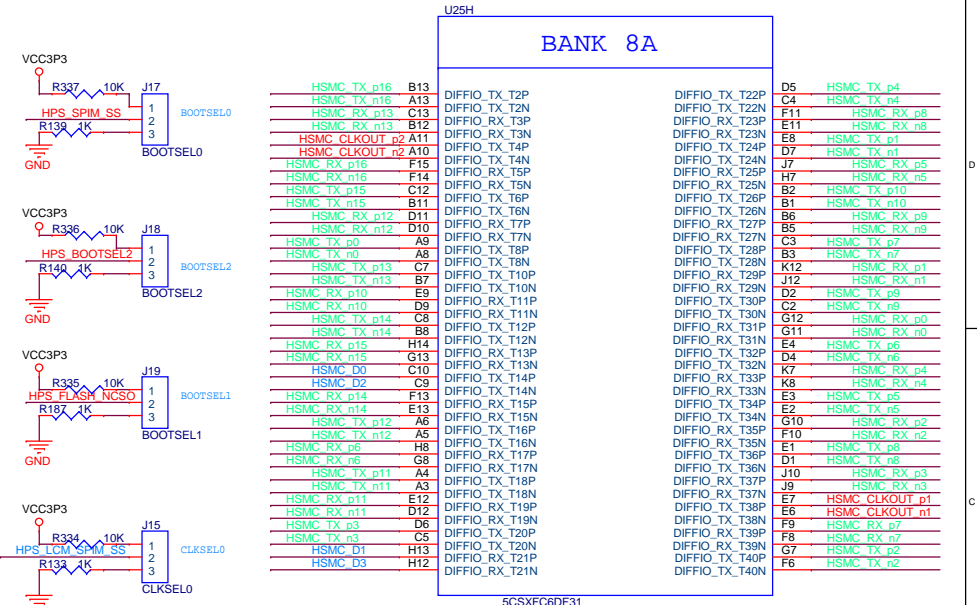
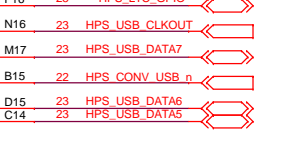
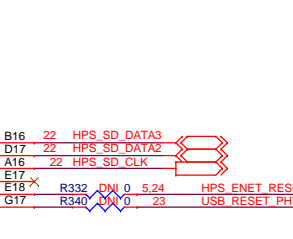
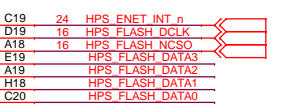
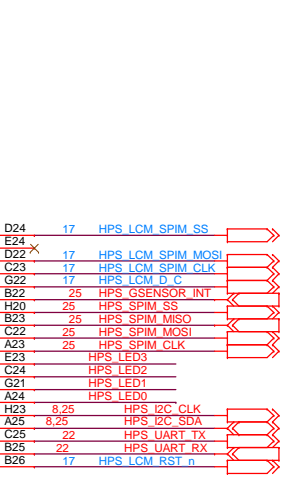
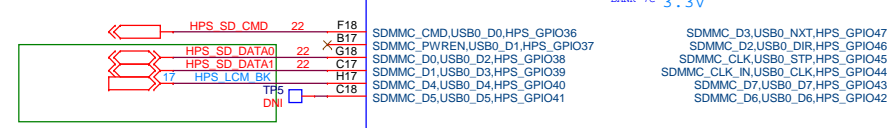
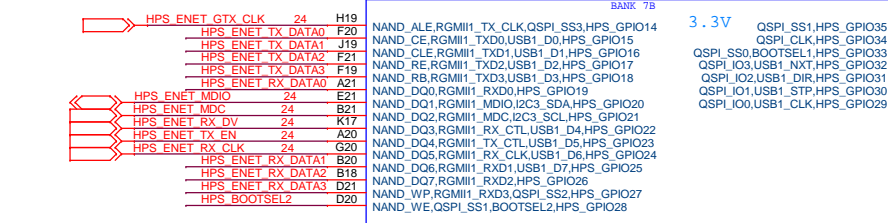
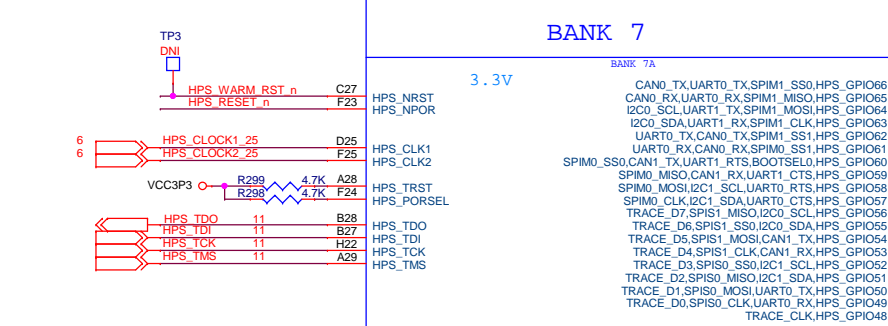
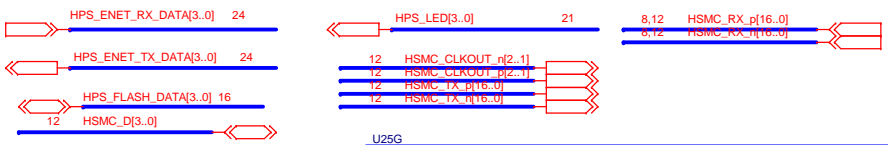


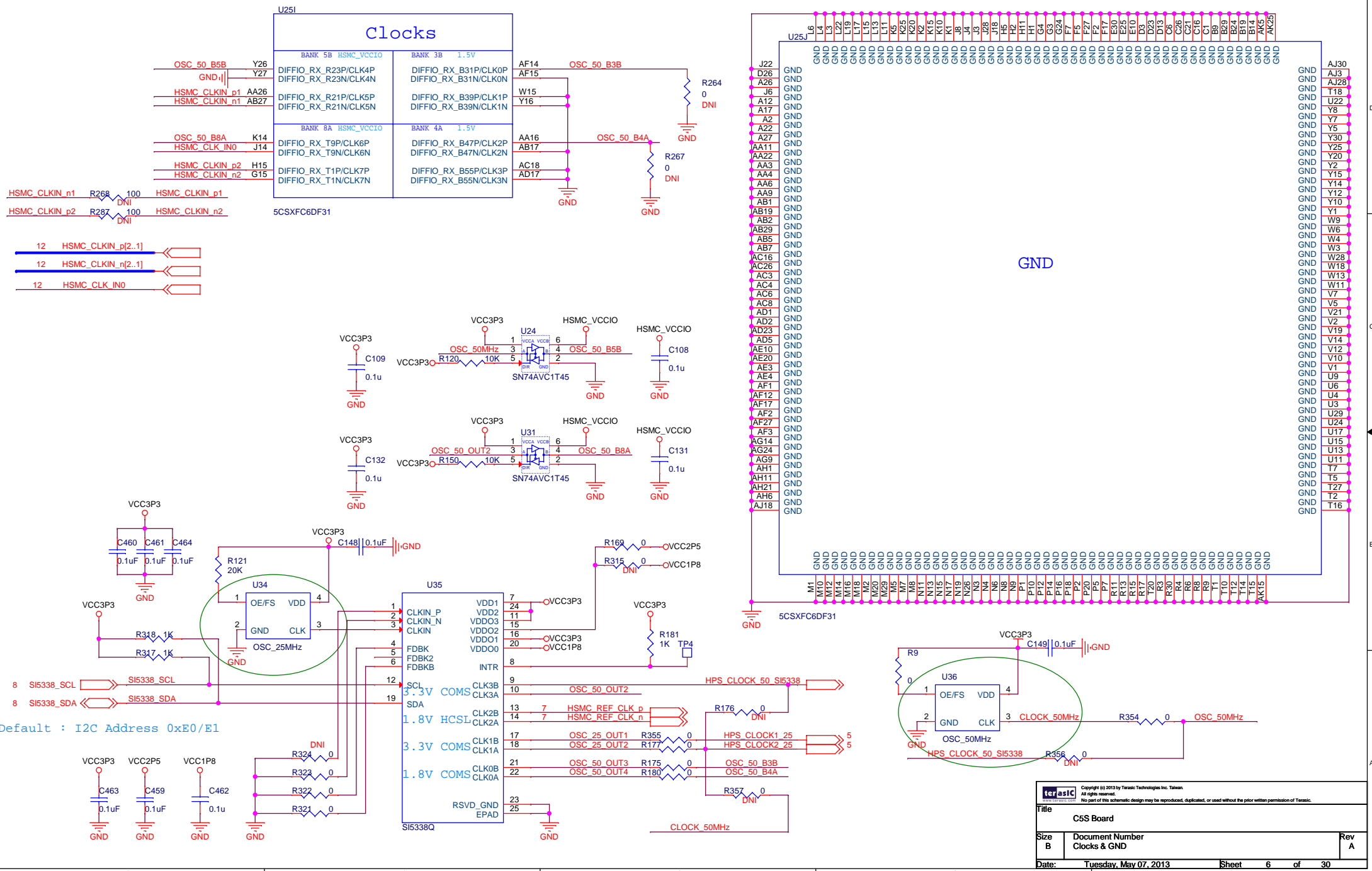
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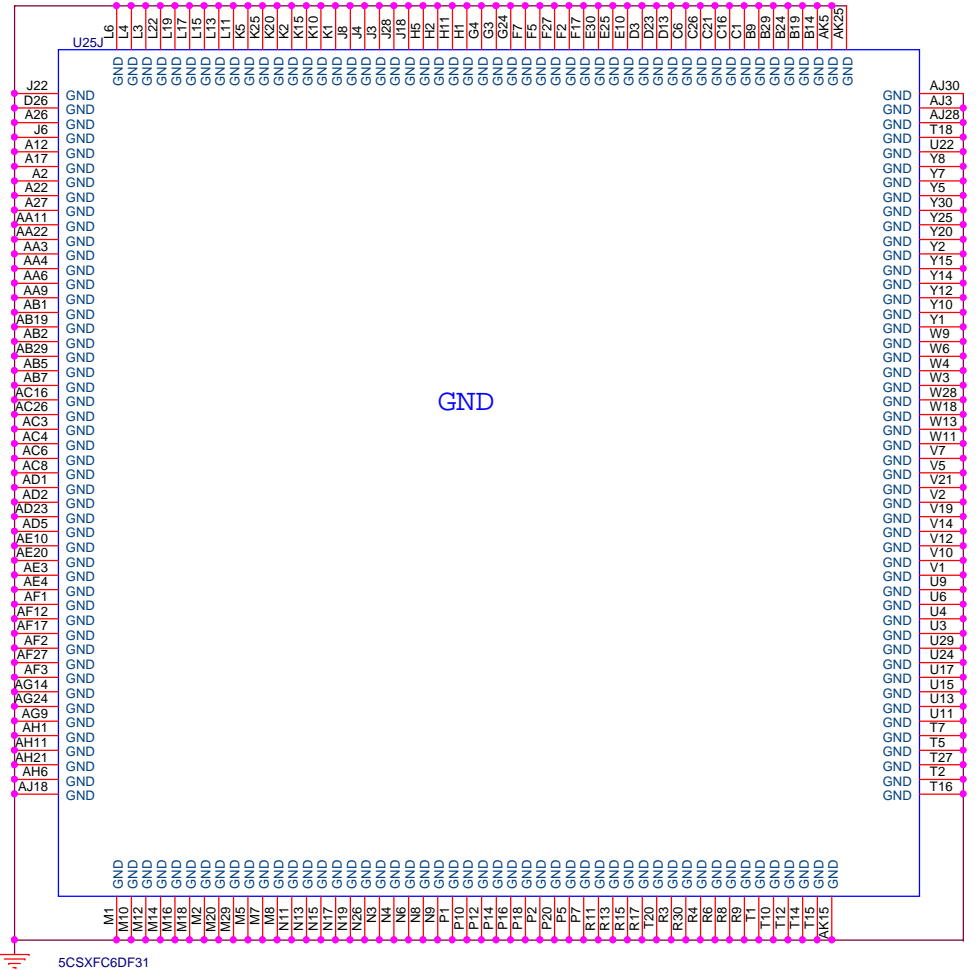
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Title		
C5S Board		
Size	Document Number	Rev
B	BANK3 & BANK4	A
Date:	Tuesday, May 07, 2013	Sheet 3 of 30







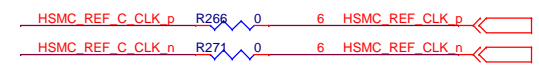
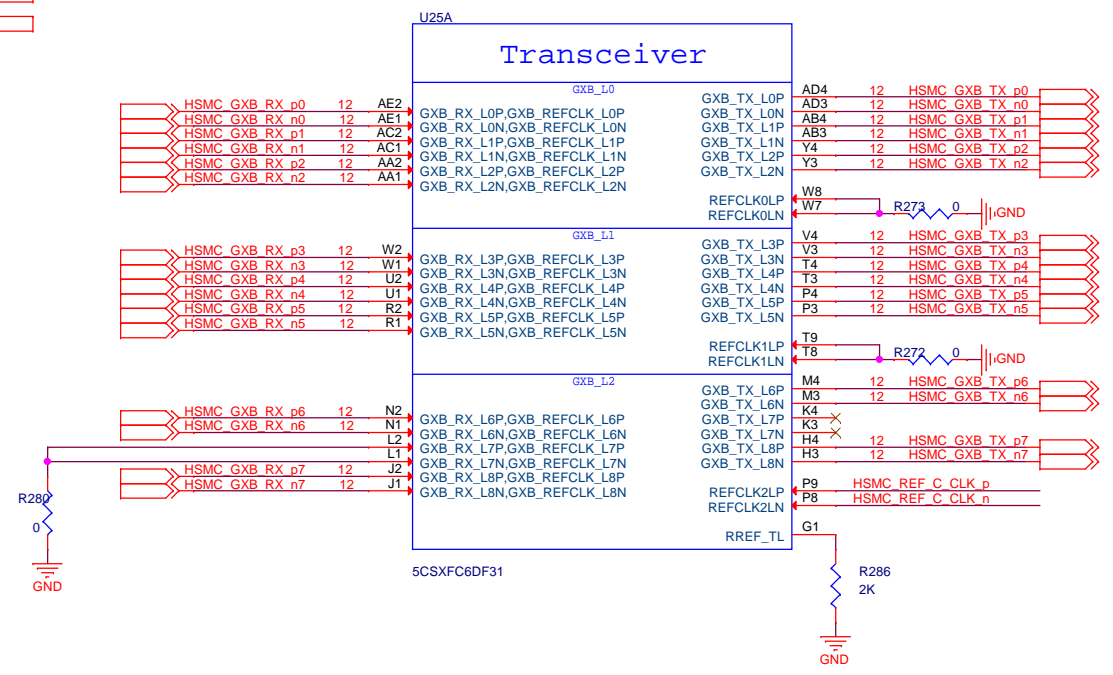
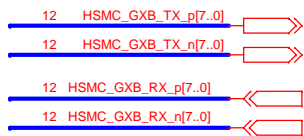
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DIFFIO_RX_R21P/CLK5P	DIFFIO_RX_R21N/CLK5N	DIFFIO_RX_B39P/CLK1P	DIFFIO_RX_B39N/CLK1N
BANK 8A HSMC_VCCIO		BANK 4A 1.5V	
DIFFIO_RX_T9P/CLK6P	DIFFIO_RX_T9N/CLK6N	DIFFIO_RX_B47P/CLK2P	DIFFIO_RX_B47N/CLK2N
DIFFIO_RX_T1P/CLK7P	DIFFIO_RX_T1N/CLK7N	DIFFIO_RX_B55P/CLK3P	DIFFIO_RX_B55N/CLK3N



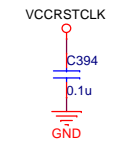
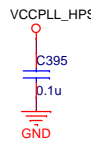
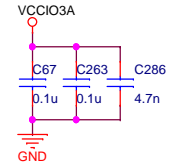
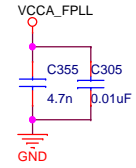
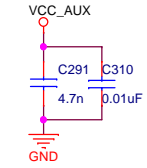
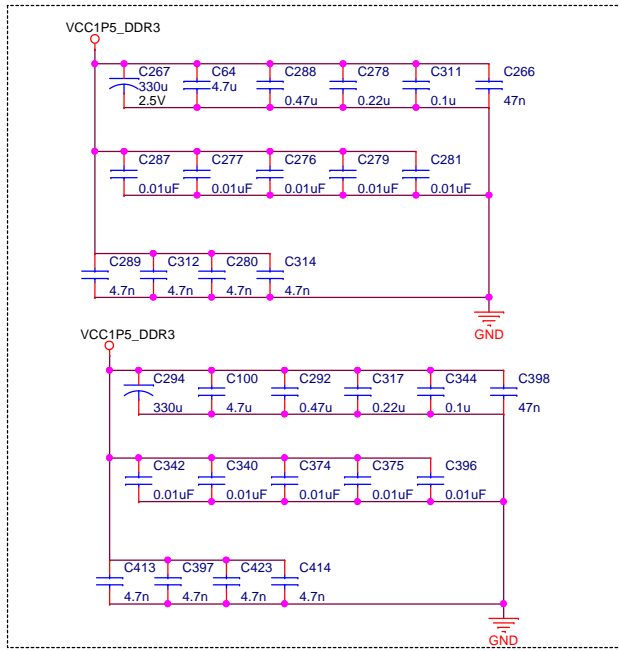
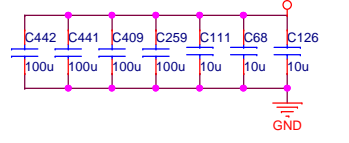
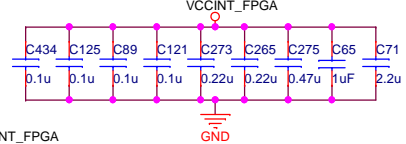
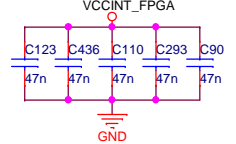
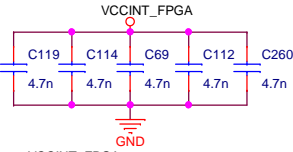
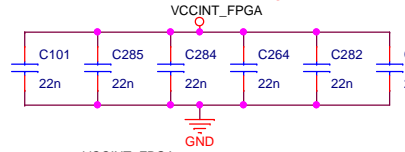
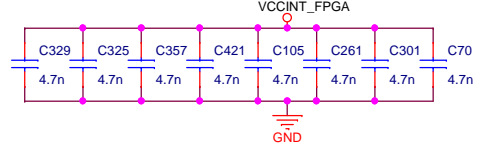
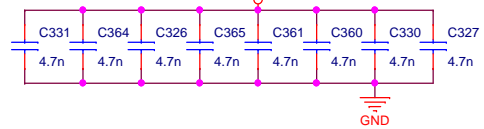
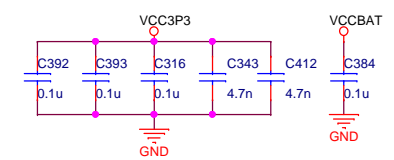
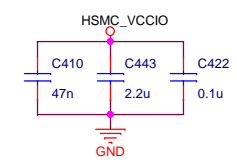
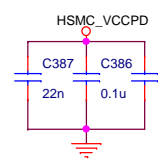
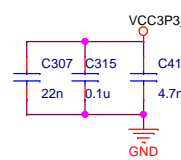
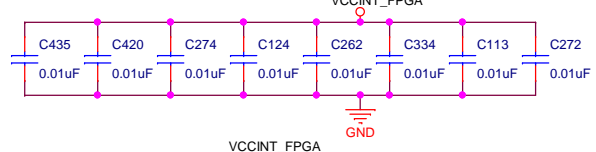
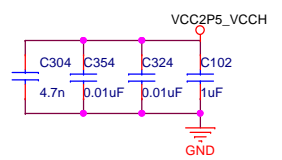
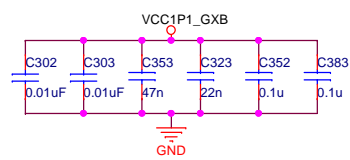
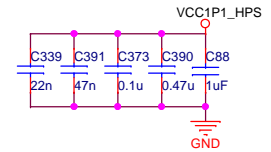
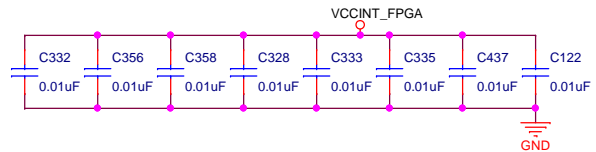
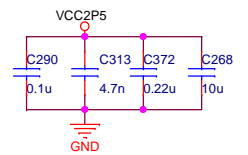
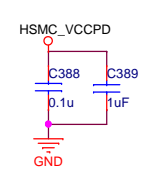
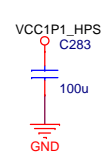
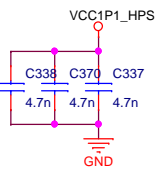
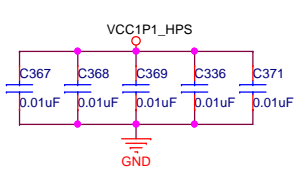
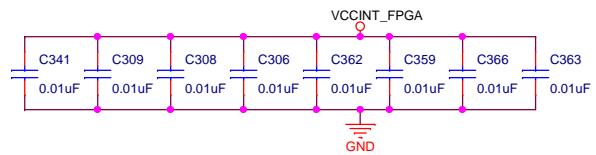
GND

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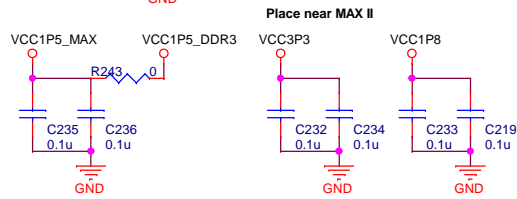
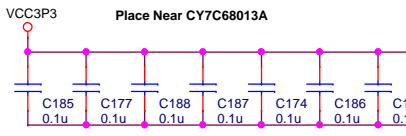
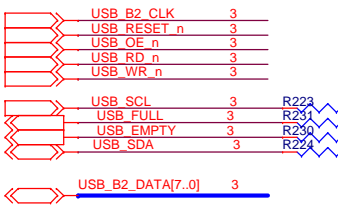
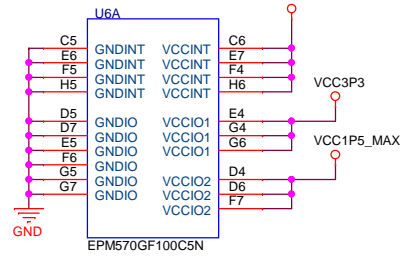
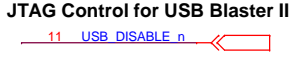
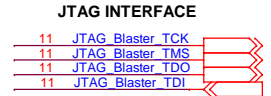
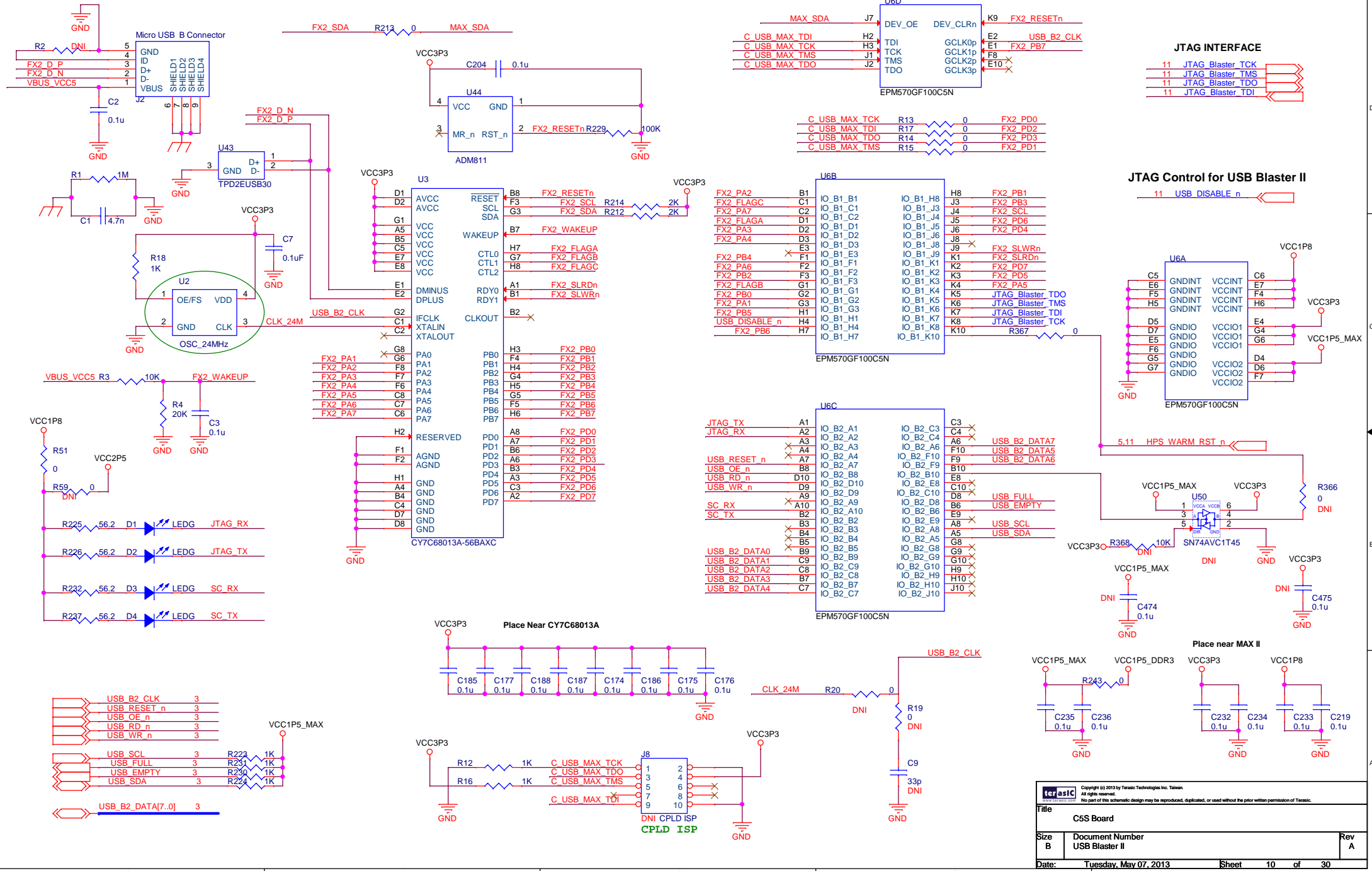
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Title		
C5S Board		
Size	Document Number	Rev
B	Clocks & GND	A
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Title C5S Board		
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Date:	Tuesday, May 07, 2013	Sheet 7 of 30

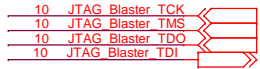


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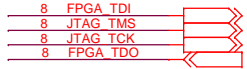


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Title: C5S Board					
Size: B	Document Number: USB Blaster II				Rev: A
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USB Blaster



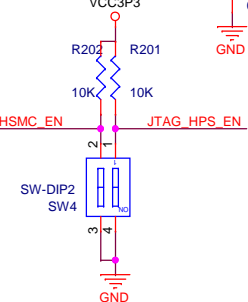
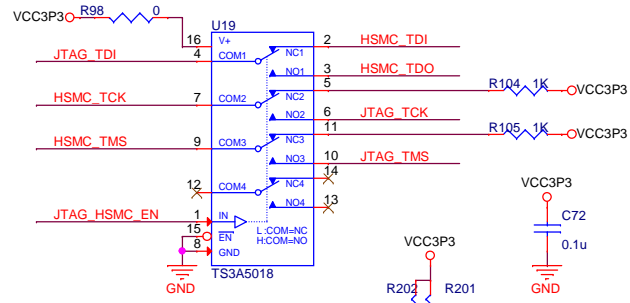
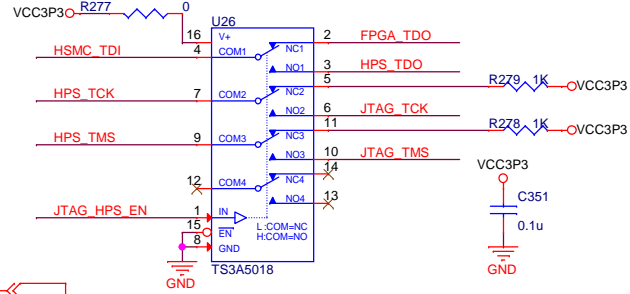
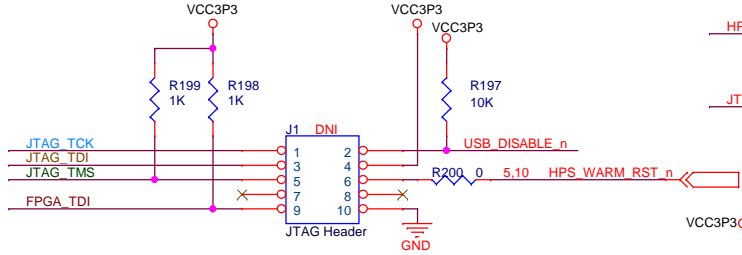
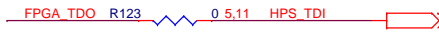
FPGA JTAG INTERFACE



HSMC JTAG INTERFACE



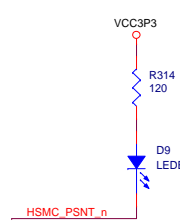
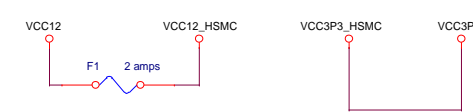
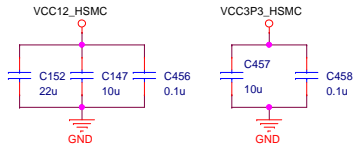
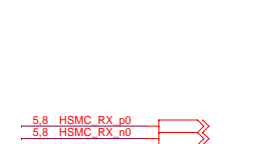
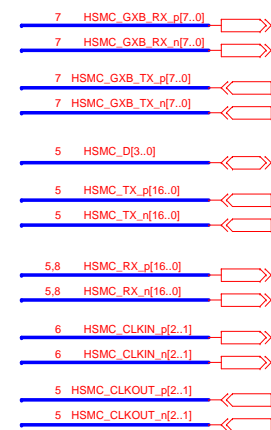
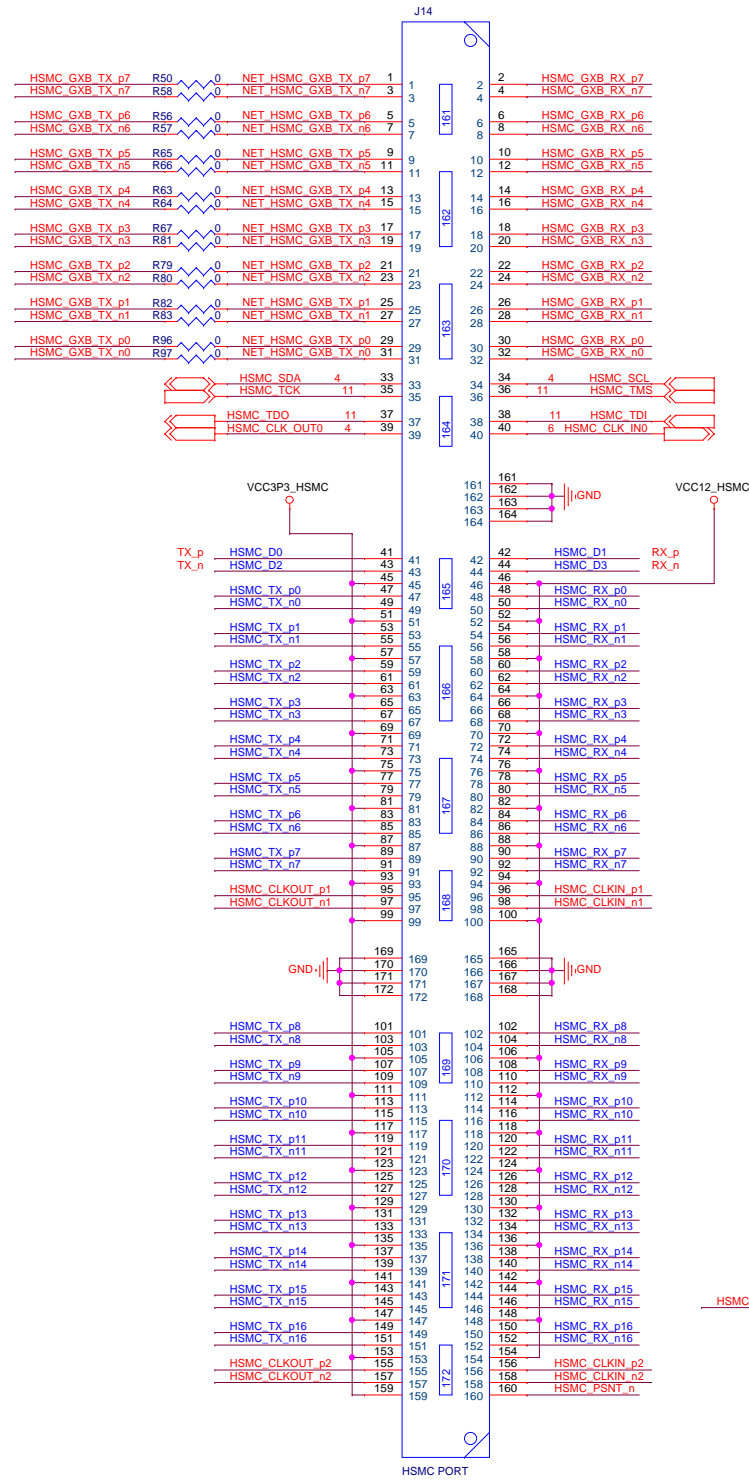
HPS JTAG INTERFACE



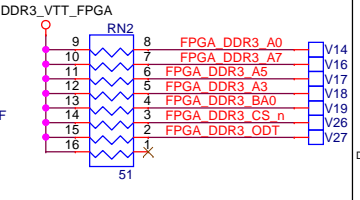
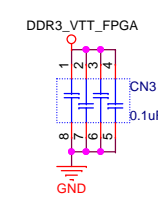
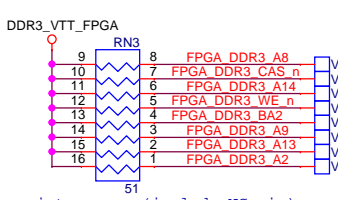
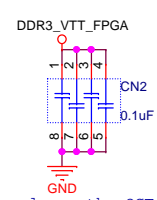
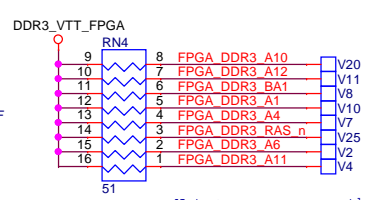
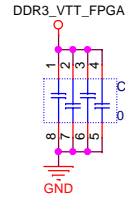
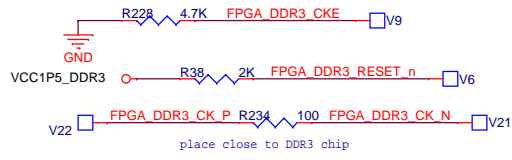
Default Disable (switch OFF)

OFF = in-chain
ON = not-in-chain

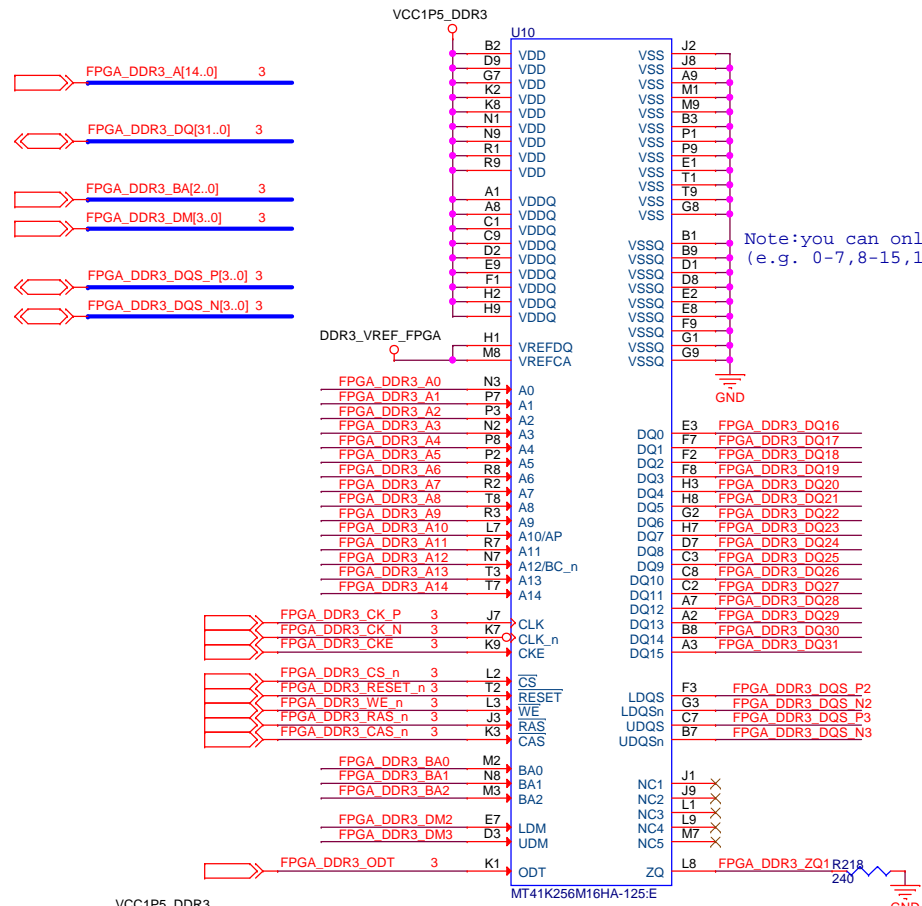
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Title: C5S Board		
Size: B	Document Number: JTAG Chain	Rev: A
Date: Tuesday, May 07, 2013	Sheet: 11	of 30



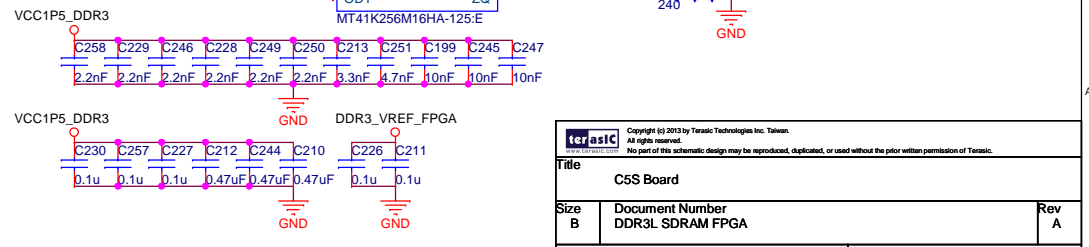
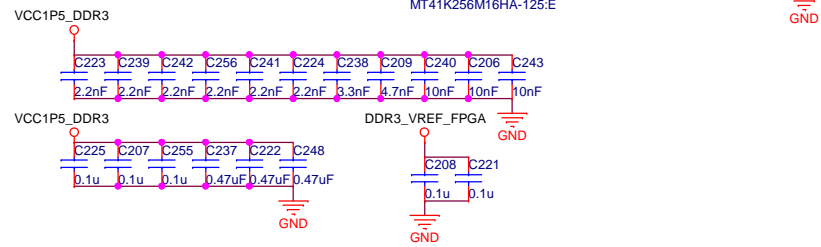
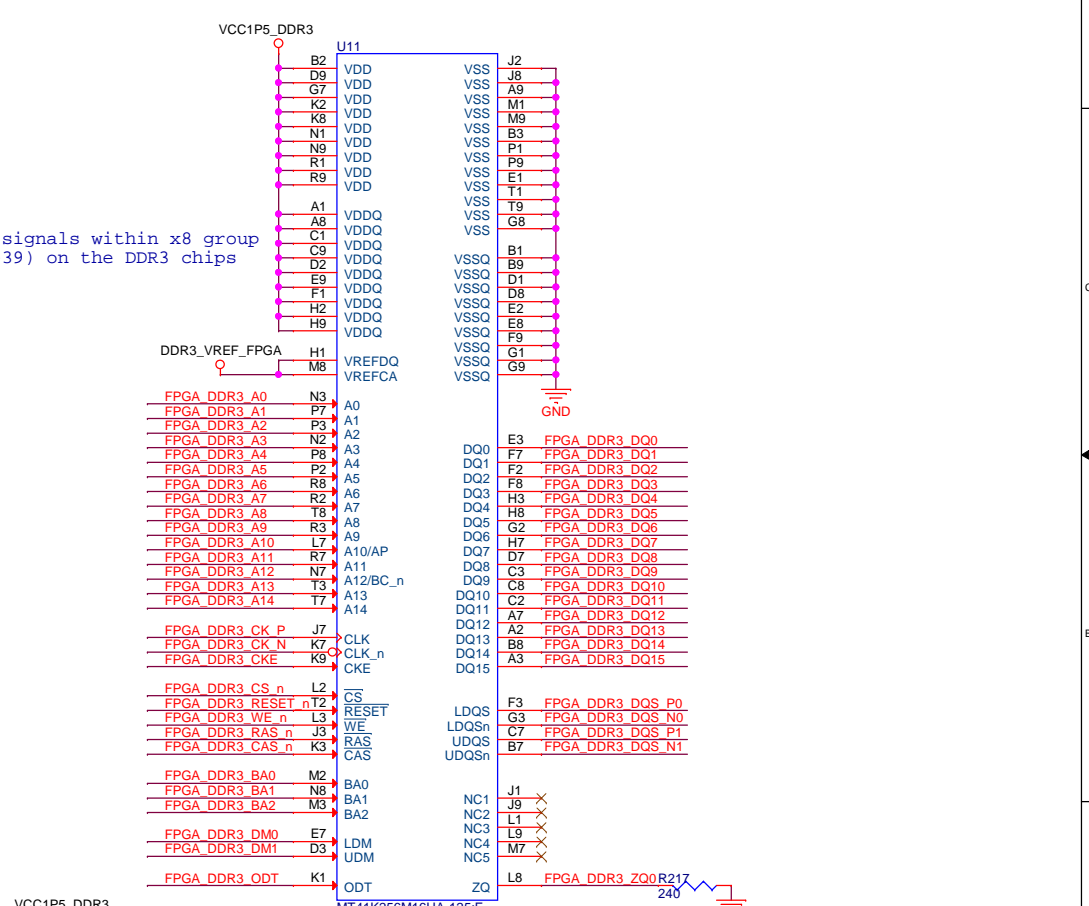
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Title: C5S Board	
Size: CustpmHSMC	Document Number: Rev A
Date: Tuesday, May 07, 2013	Sheet 12 of 30



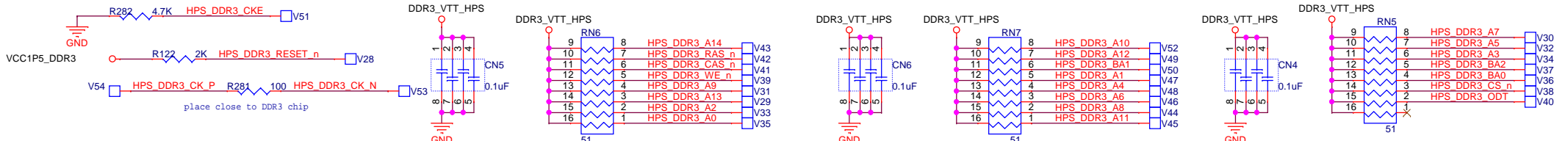
Note: you can swap the signals on the OCT resistor array (include NC pin)



Note: you can only swap the DQ signals within x8 group (e.g. 0-7, 8-15, 16-23, 24-31, 32-39) on the DDR3 chips

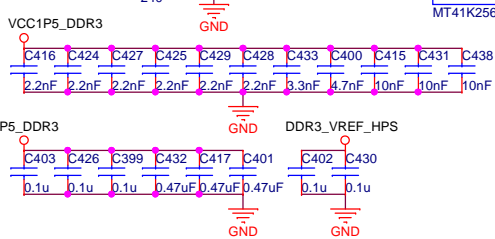
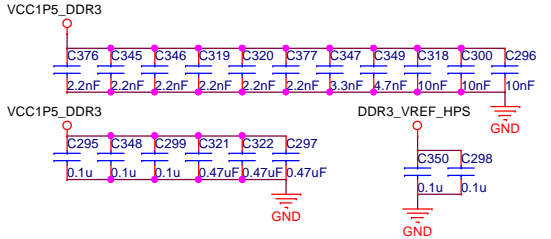
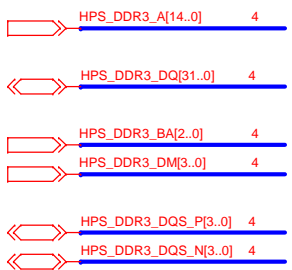


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Title		
C5S Board		
Size	Document Number	Rev
B	DDR3L SDRAM FPGA	A
Date:	Tuesday, May 07, 2013	Sheet 13 of 30

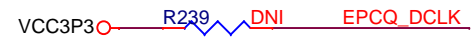
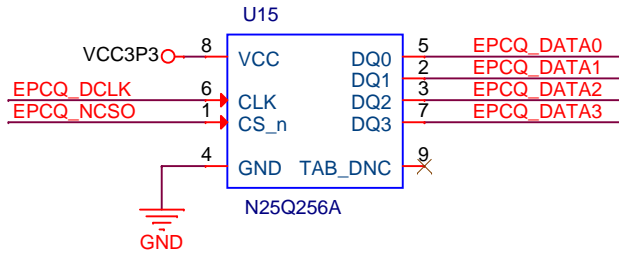
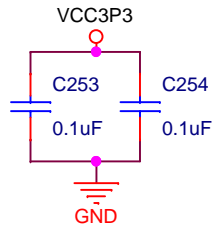
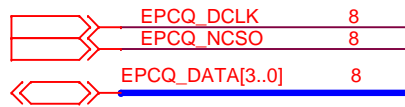



Note: you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31) on the DDR3 chips

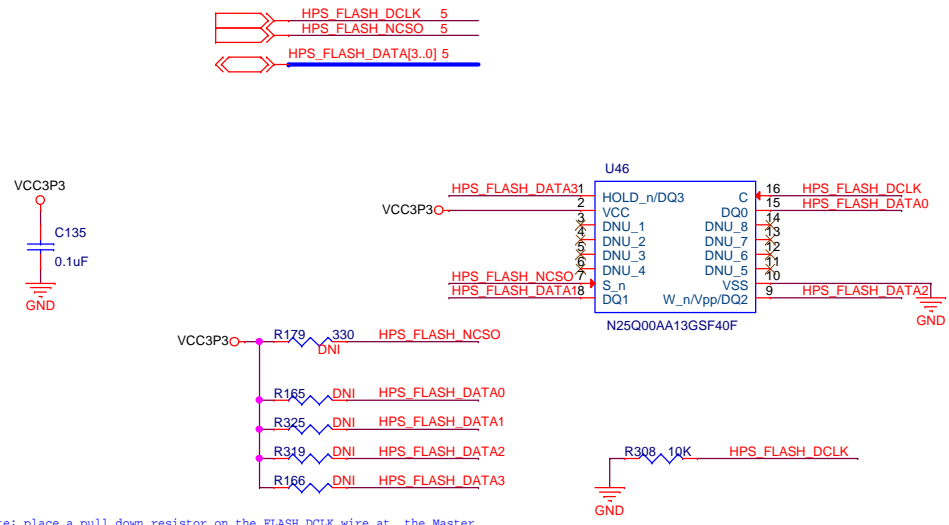
Note: you can swap the signals on the OCT resistor array(include NC pin)




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Title	
C5S Board	
Size	Document Number
B	DDR3L SDRAM HPS
Date:	Tuesday, May 07, 2013
Sheet	14 of 30
Rev	A



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Title C5S Board		
Size A	Document Number EPCQ	Rev A
Date: Tuesday, May 07, 2013		
Sheet 15		of 30



Note: place a pull down resistor on the FLASH_DCLK wire at the Master

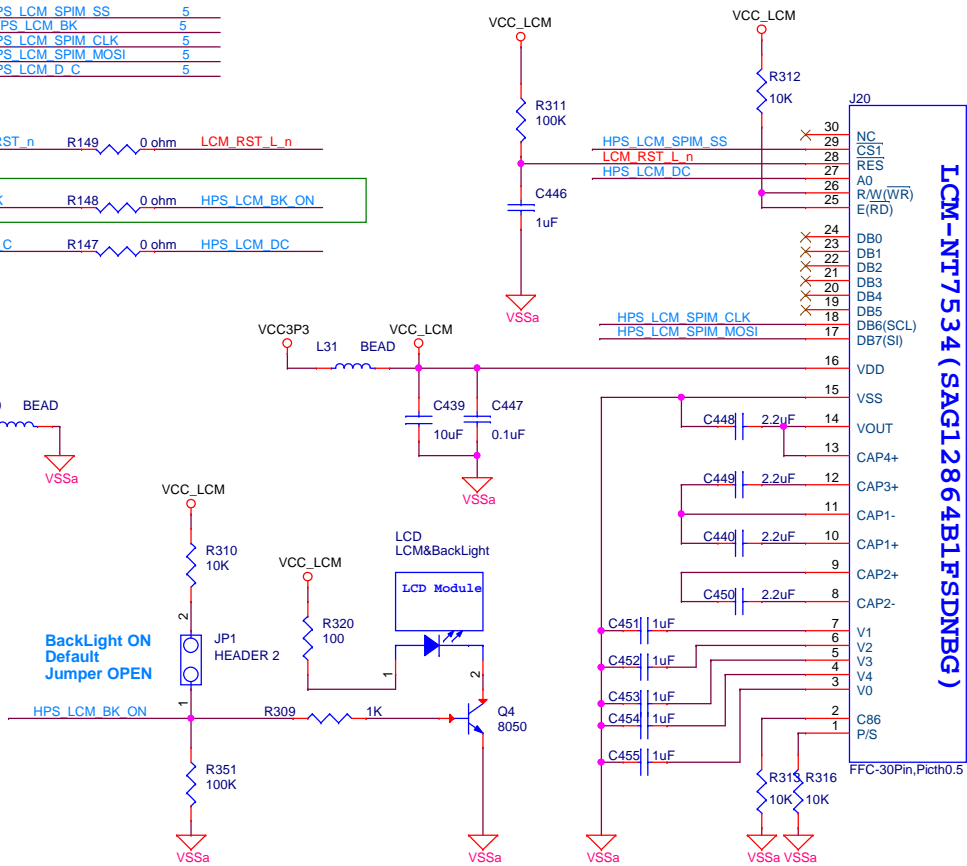
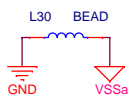
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Title		
C5S Board		
Size	Document Number	Rev
B	QSPI FLASH HPS	A
Date:	Tuesday, May 07, 2013	Sheet 16 of 30

- HPS_LCM_RST_n 5
- HPS_LCM_SPIM_SS 5
- HPS_LCM_BK 5
- HPS_LCM_SPIM_CLK 5
- HPS_LCM_SPIM_MOSI 5
- HPS_LCM_D_C 5

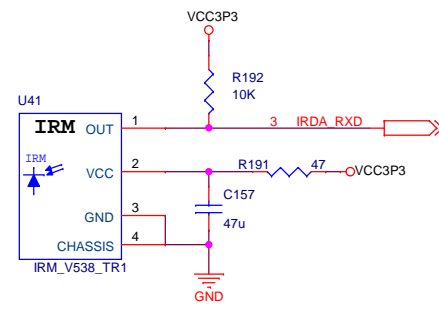
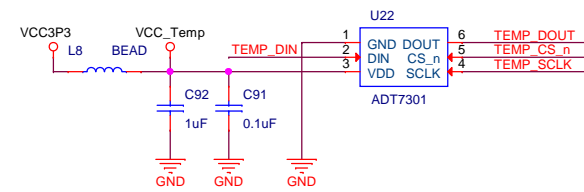
HPS_LCM_RST_n R149 0 ohm LCM_RST_L_n

HPS_LCM_BK R148 0 ohm HPS_LCM_BK_ON

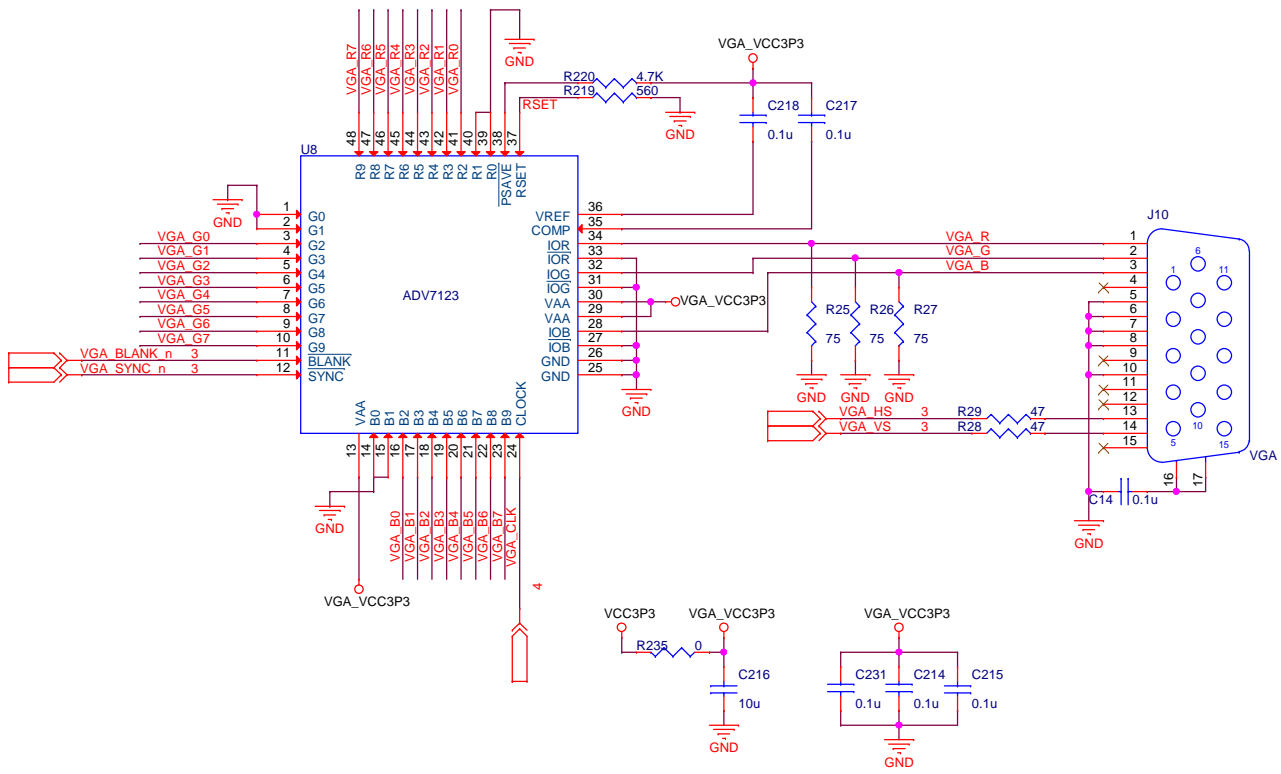
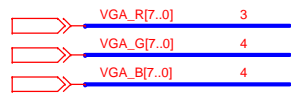
HPS_LCM_D_C R147 0 ohm HPS_LCM_DC



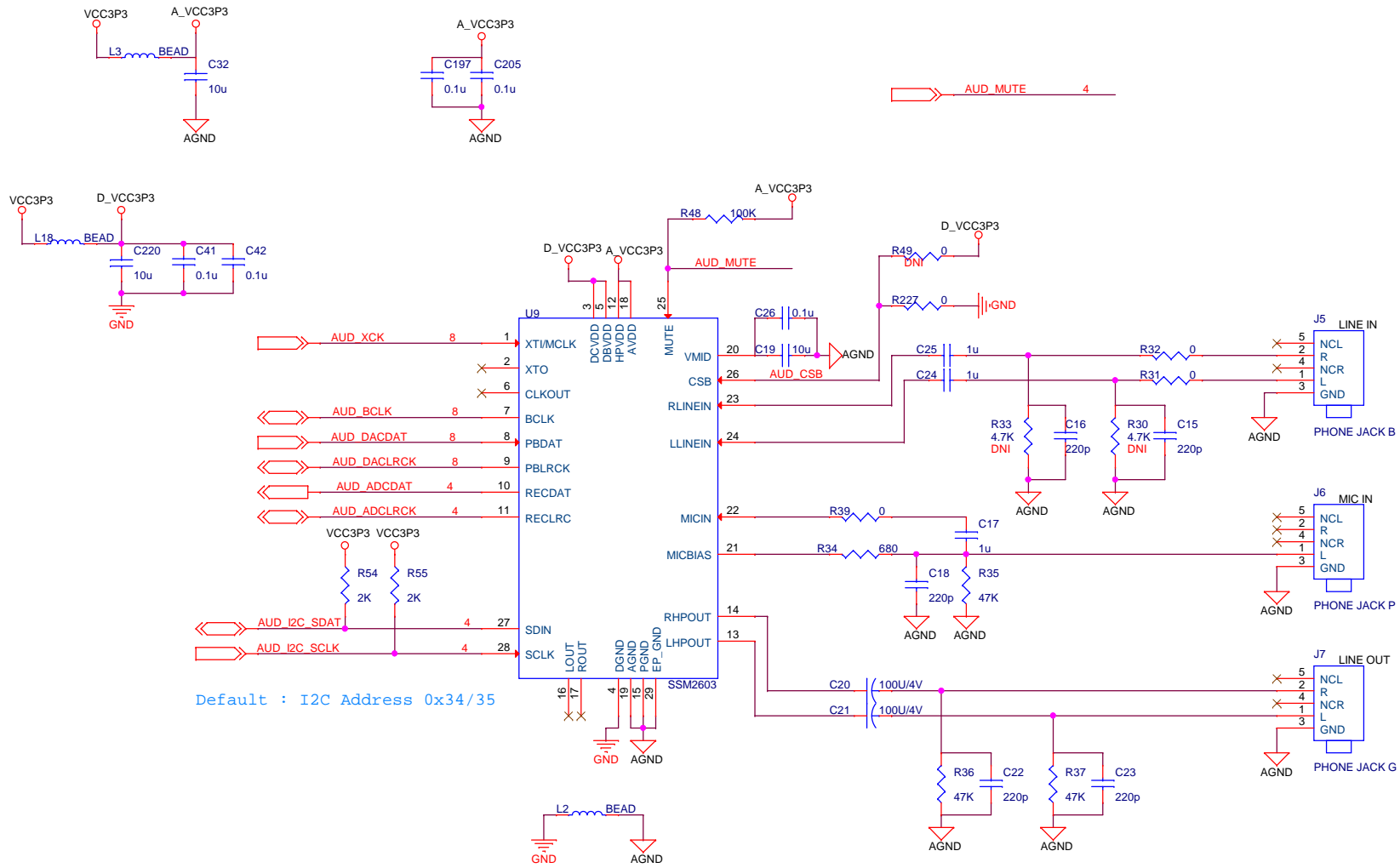
- TEMP_SCLK 3
- TEMP_CS_n 3
- TEMP_DIN 3
- TEMP_DOUT 3




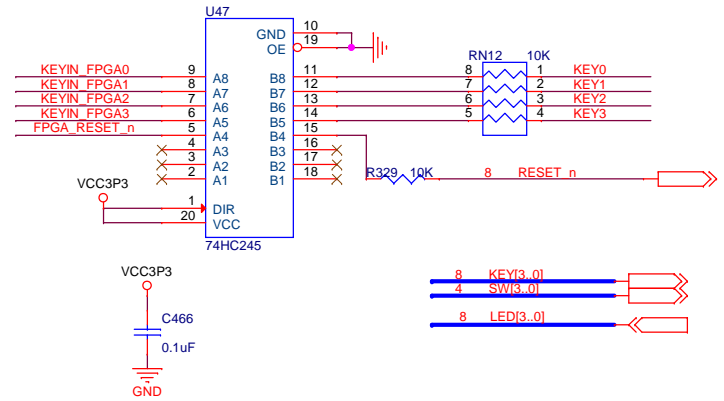
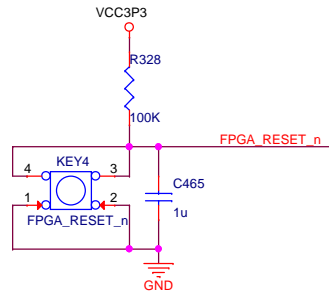
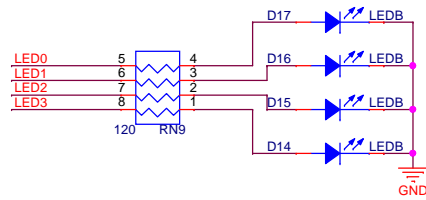
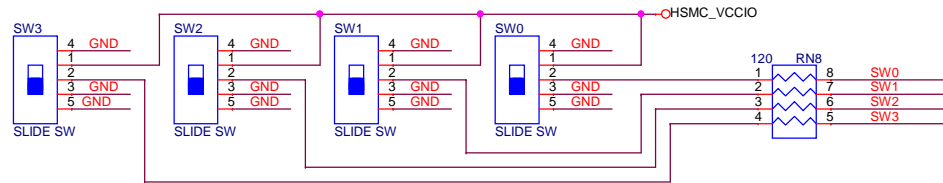
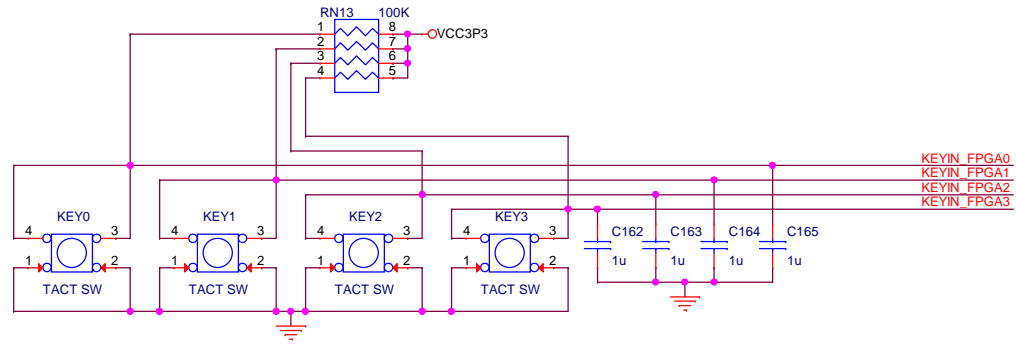
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Title		
C5S Board		
Size	Document Number	Rev
B	LCD & Temp sensor & IRM	A
Date:	Tuesday, May 07, 2013	Sheet 17 of 30

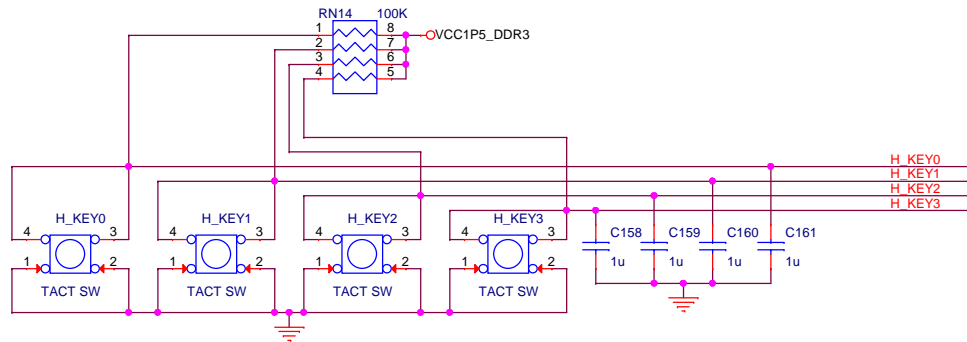


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Title		
C5S Board		
Size	Document Number	Rev
B	VGA ADV7123	A
Date:	Tuesday, May 07, 2013	Sheet 18 of 30

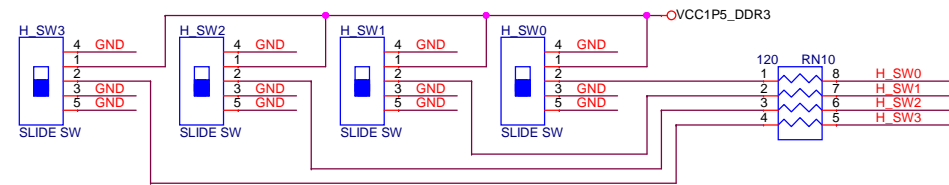


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Title		
C5S Board		
Size	Document Number	Rev
B	Audio DAC	A
Date:	Tuesday, May 07, 2013	Sheet 19 of 30

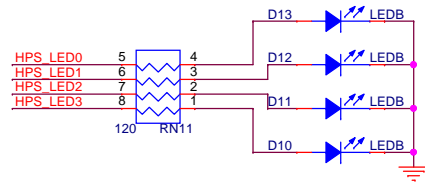
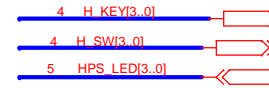
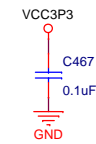




H_KEY0
H_KEY1
H_KEY2
H_KEY3

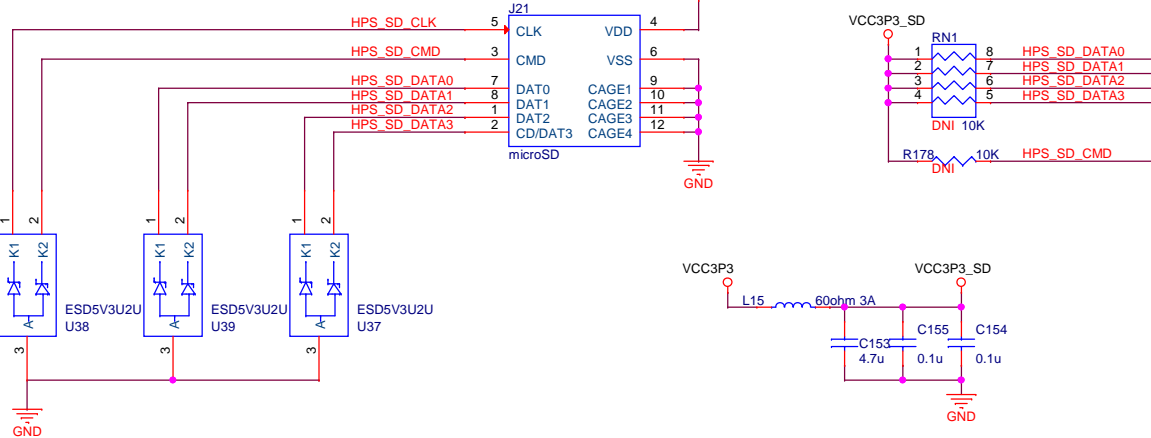
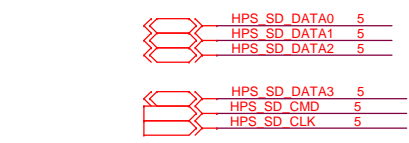
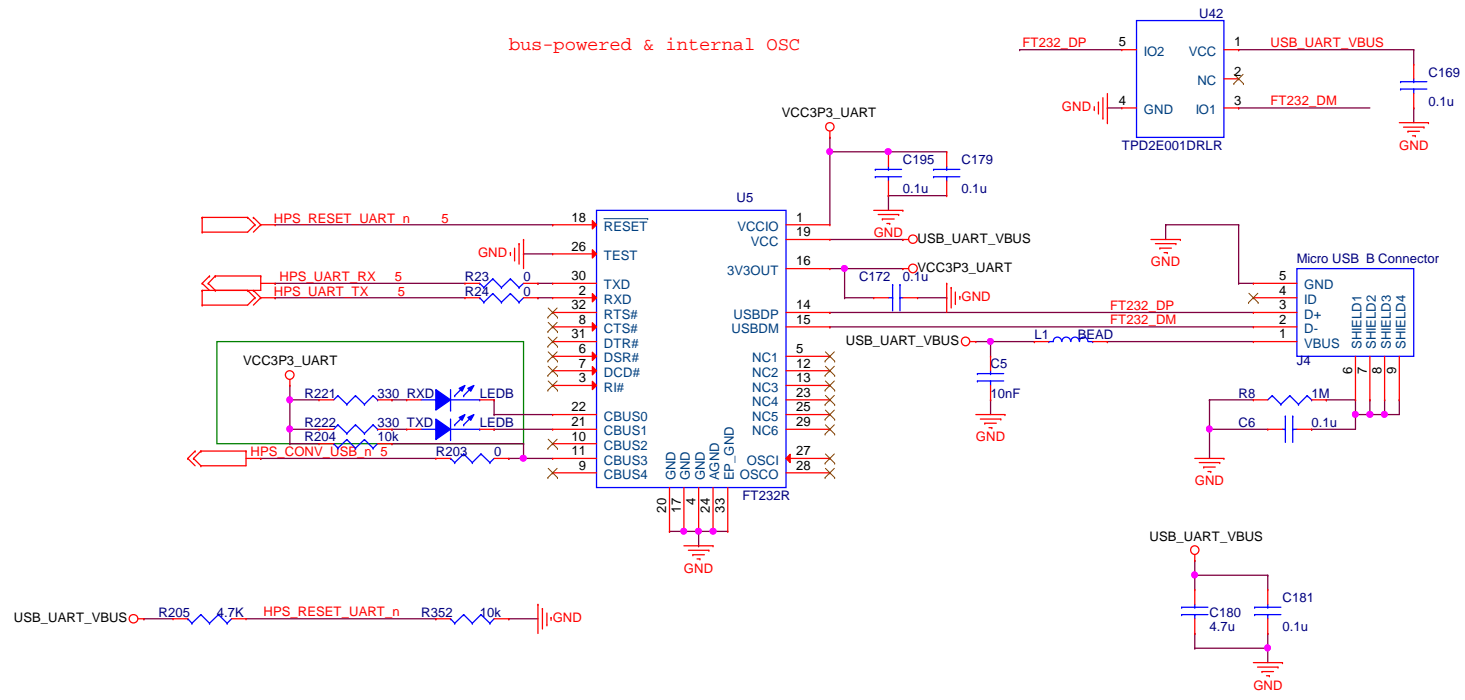


H_SW0
H_SW1
H_SW2
H_SW3

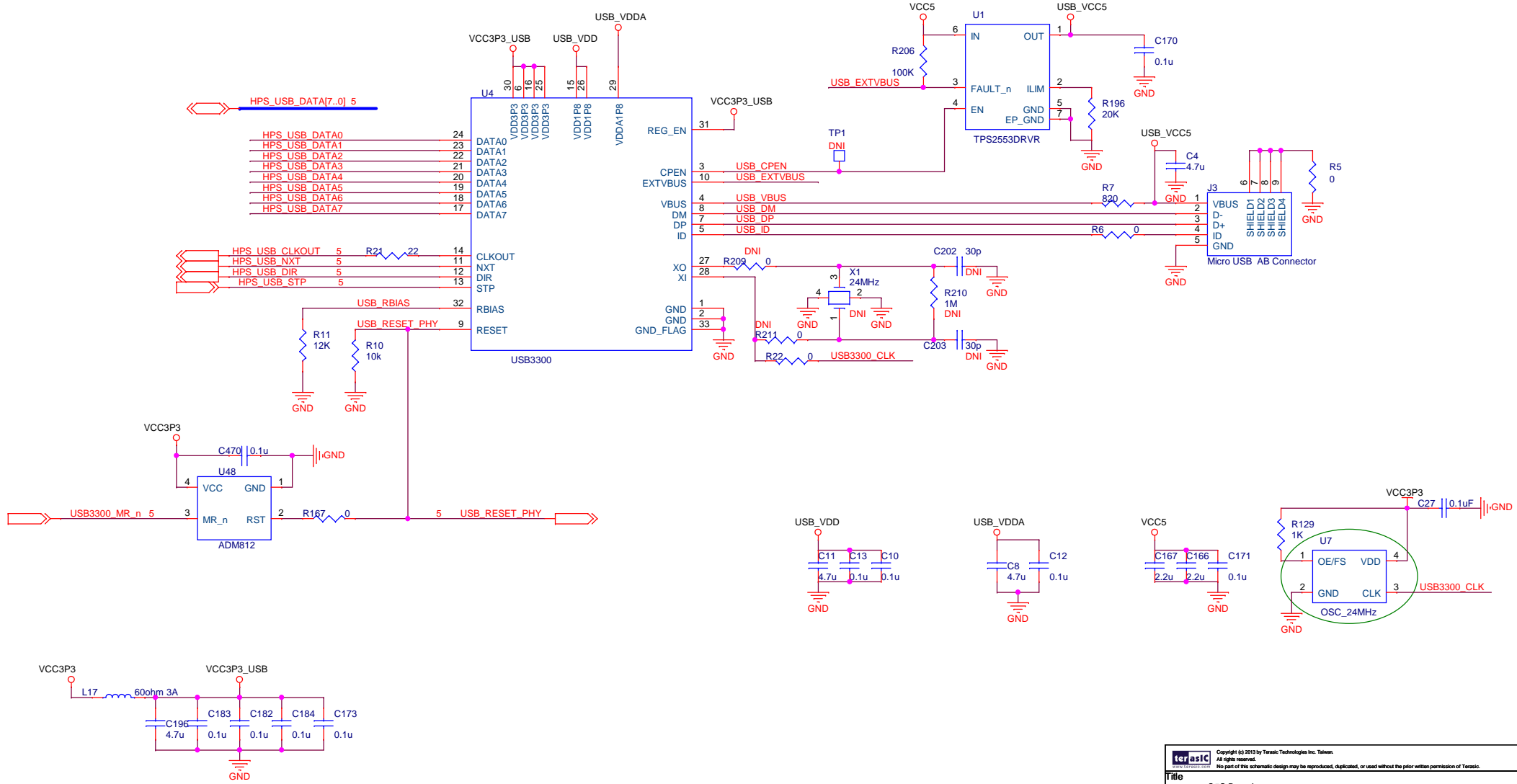


HPS_LED0
HPS_LED1
HPS_LED2
HPS_LED3

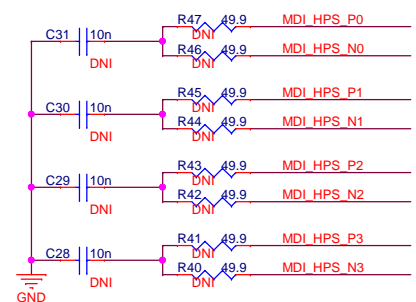
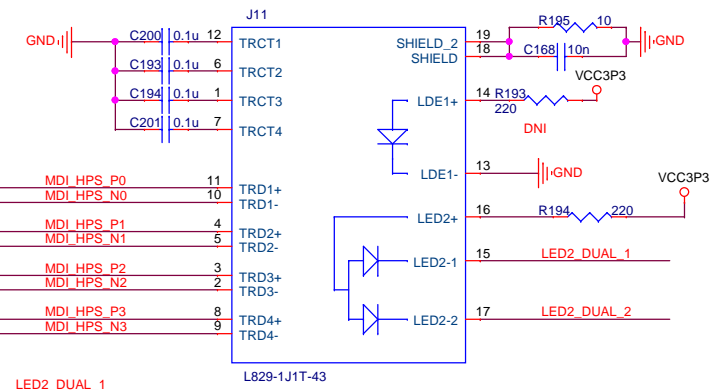
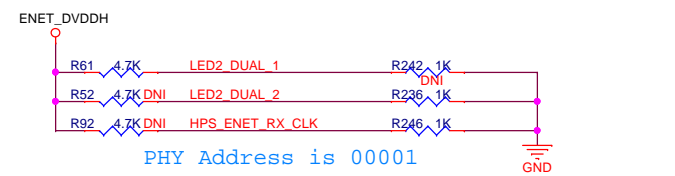
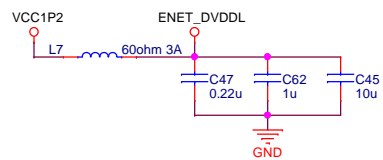
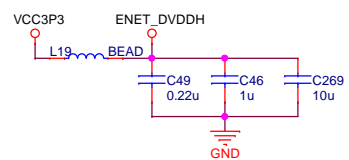
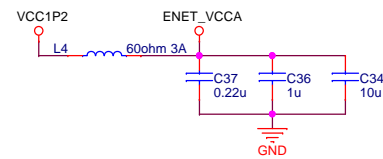
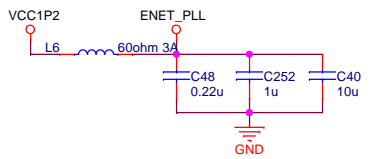
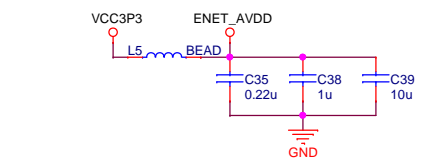
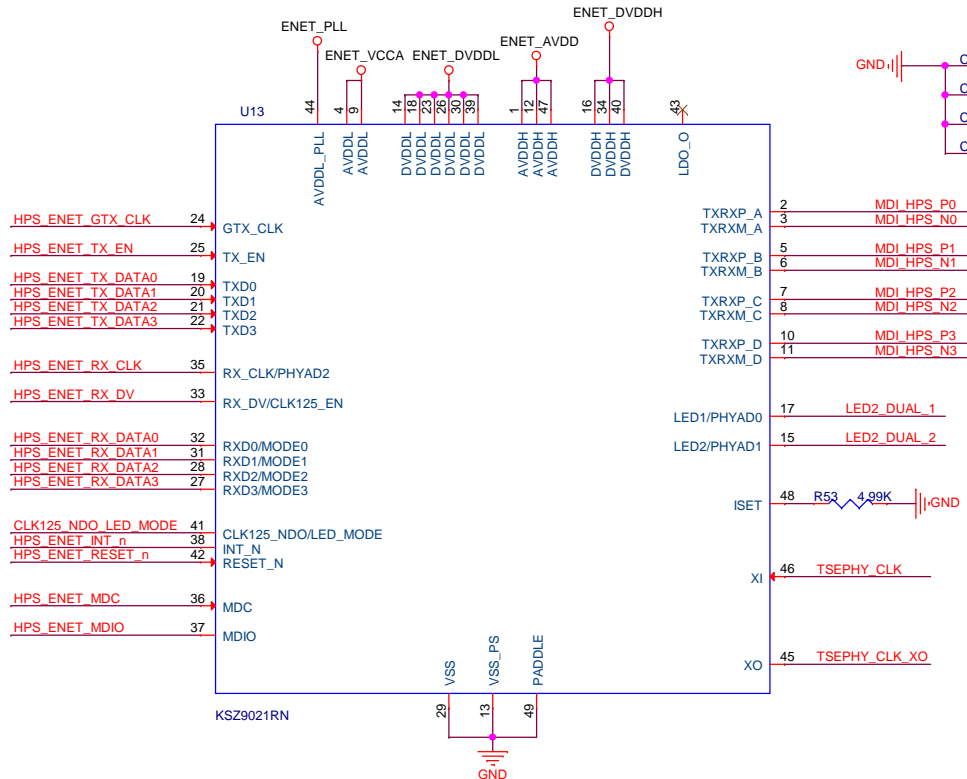
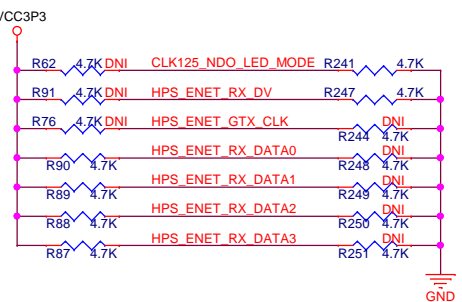
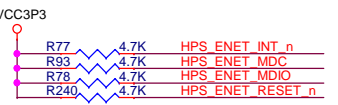
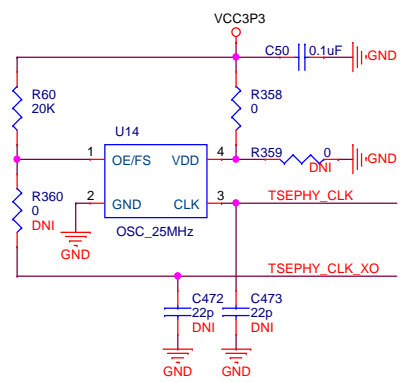
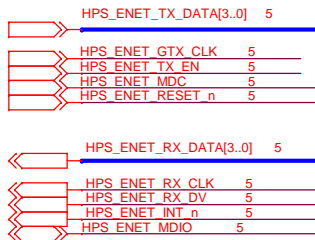
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Title	
C5S Board	
Size	Document Number
B	HPS BUTTON & SW
Date:	Tuesday, May 07, 2013
Sheet	21 of 30
Rev	A



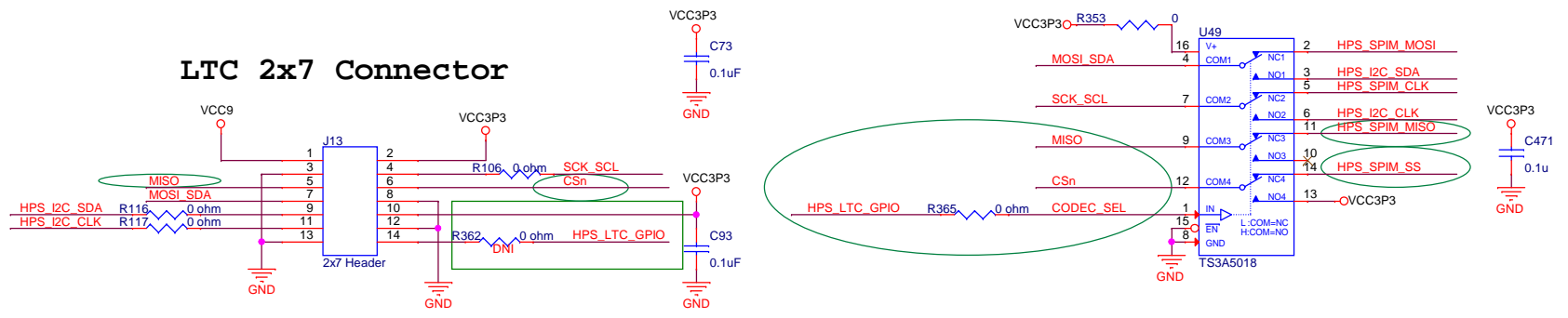
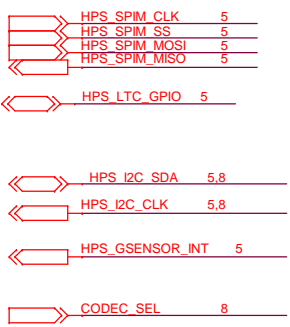
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Title		
C5S Board		
Size	Document Number	Rev
B	USB to UART & SD CARD	A
Date:	Tuesday, May 07, 2013	Sheet 22 of 30



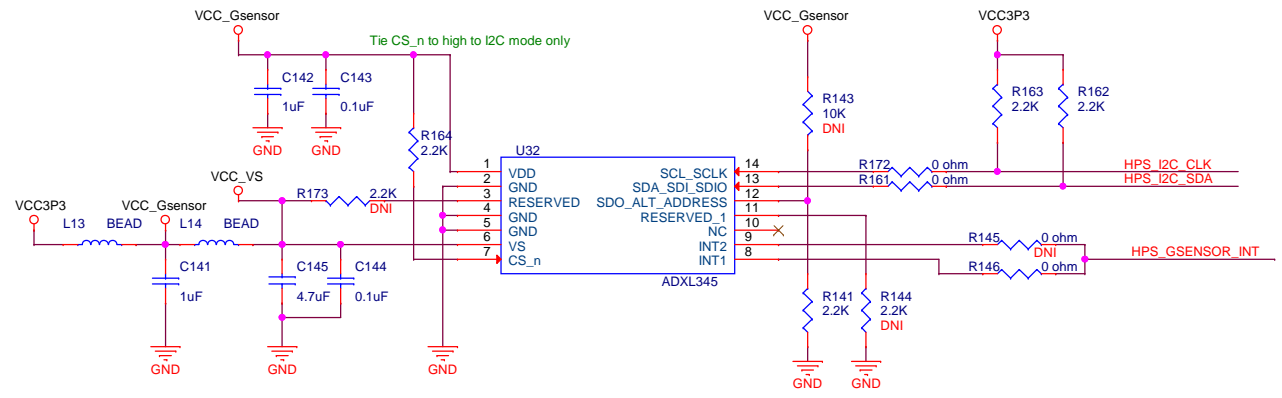
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Title		
C5S Board		
Size	Document Number	Rev
B	USB3300	A
Date:	Tuesday, May 07, 2013	Sheet 23 of 30



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Title		
C5S Board		
Size	Document Number	Rev
B	TSE PHY	A
Date:	Tuesday, May 07, 2013	Sheet 24 of 30

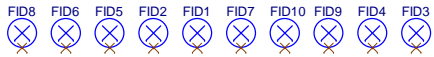
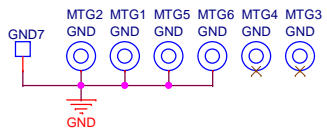


Digital Accelerometer

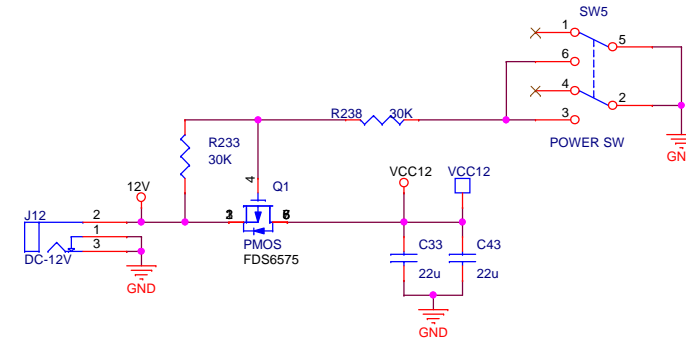
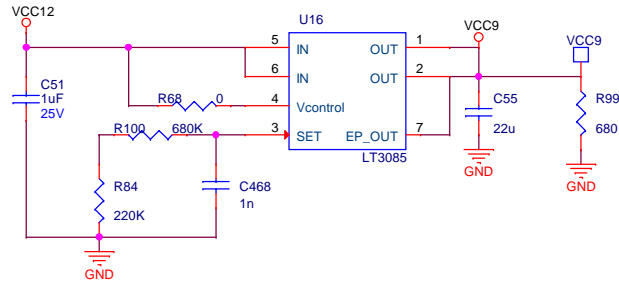


Default : I2C Address 0xA6/0xA7

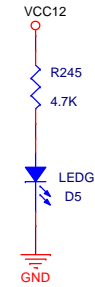
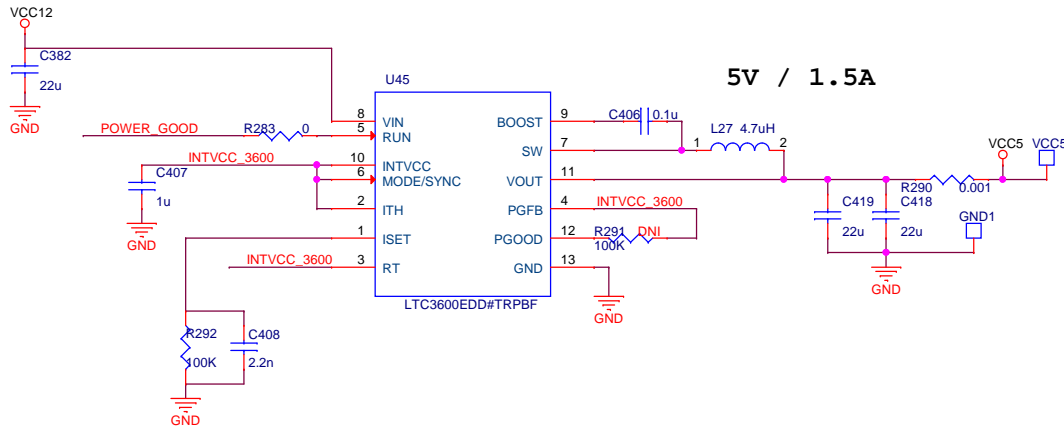
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Title		
C5S Board		
Size	Document Number	Rev
B	LTC Connector & G sensor	A
Date:	Tuesday, May 07, 2013	Sheet 25 of 30



9V / 50mA

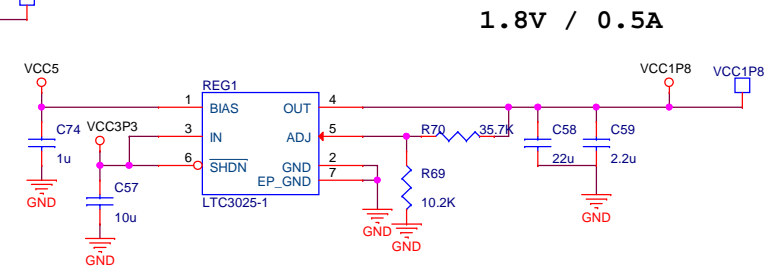
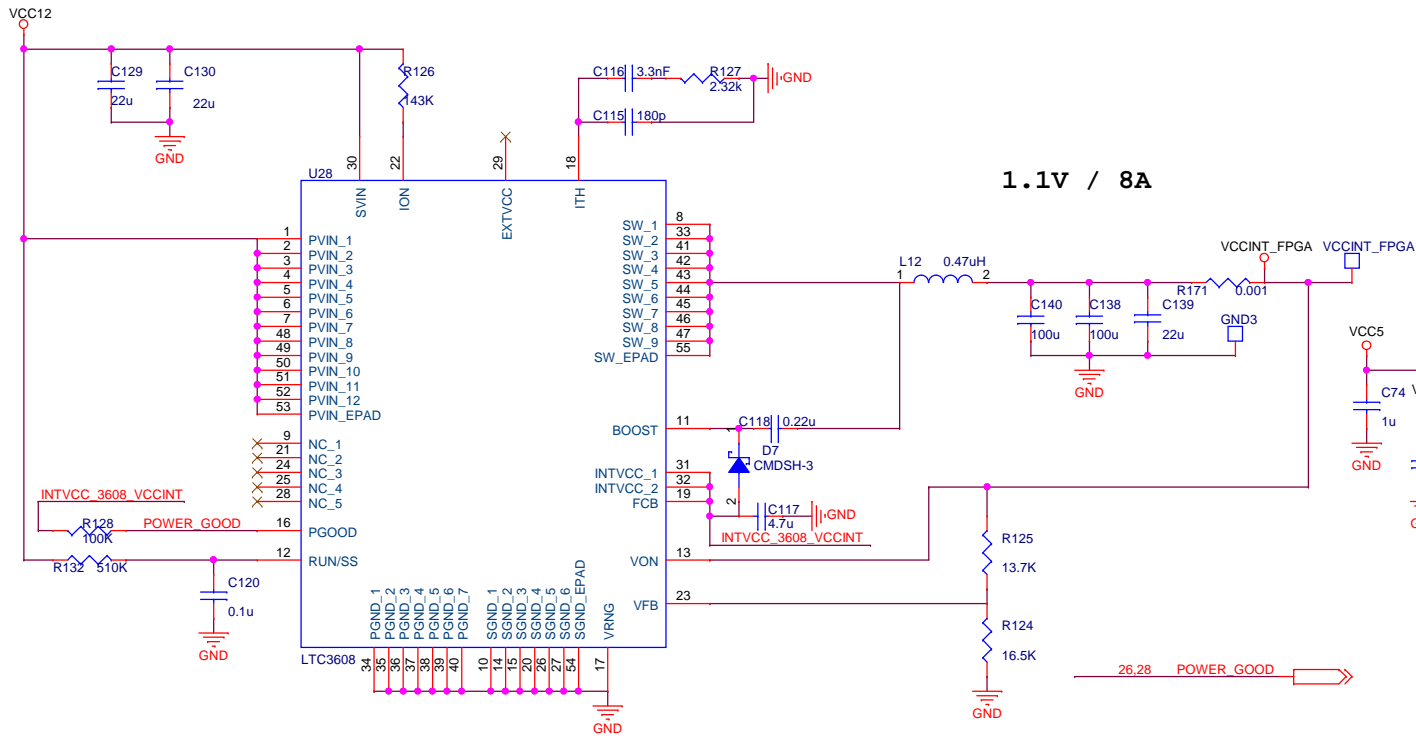
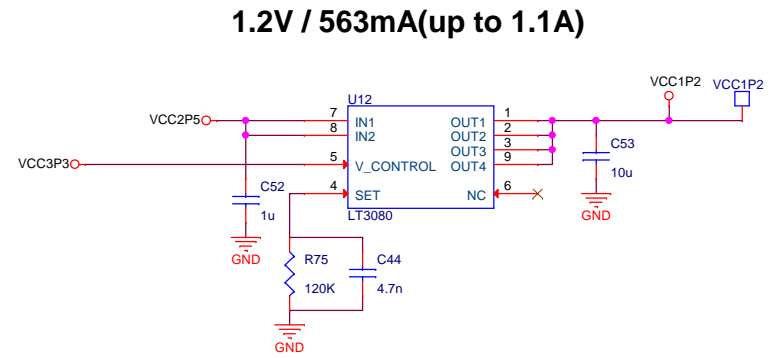
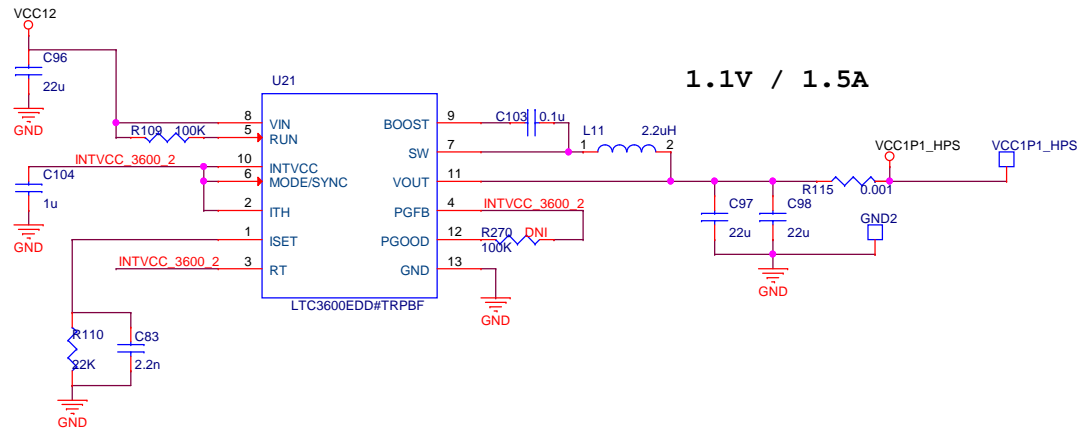


5V / 1.5A



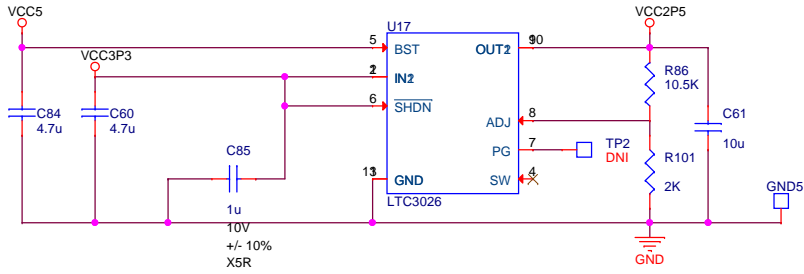
POWER_GOOD 27,28

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Title		
C5S Board		
Size	Document Number	Rev
B	Power - 9V & 5V	A
Date:	Tuesday, May 07, 2013	Sheet 26 of 30

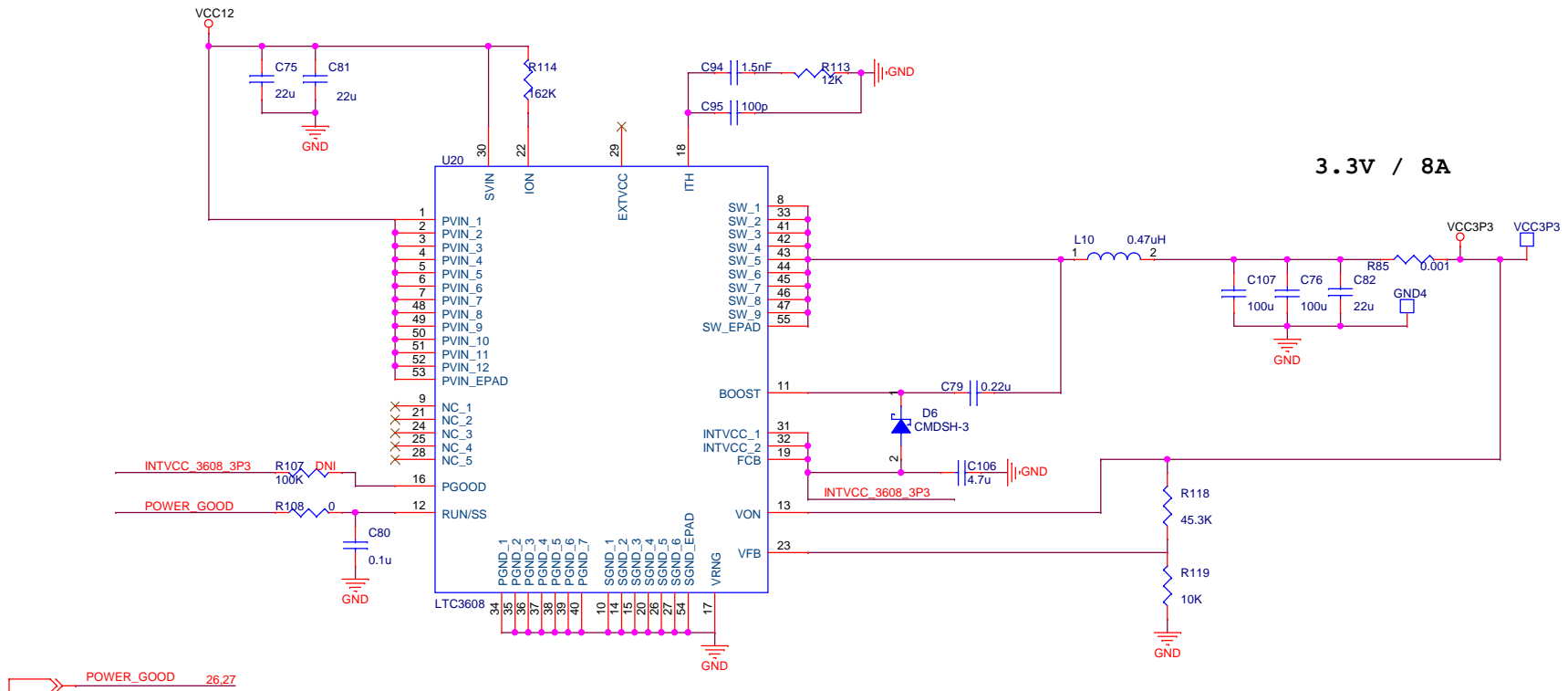


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Title		
C5S Board		
Size	Document Number	Rev
B	Power - 1.1V & 1.2V	A
Date:	Tuesday, May 07, 2013	Sheet 27 of 30

2.5V / 1.5A

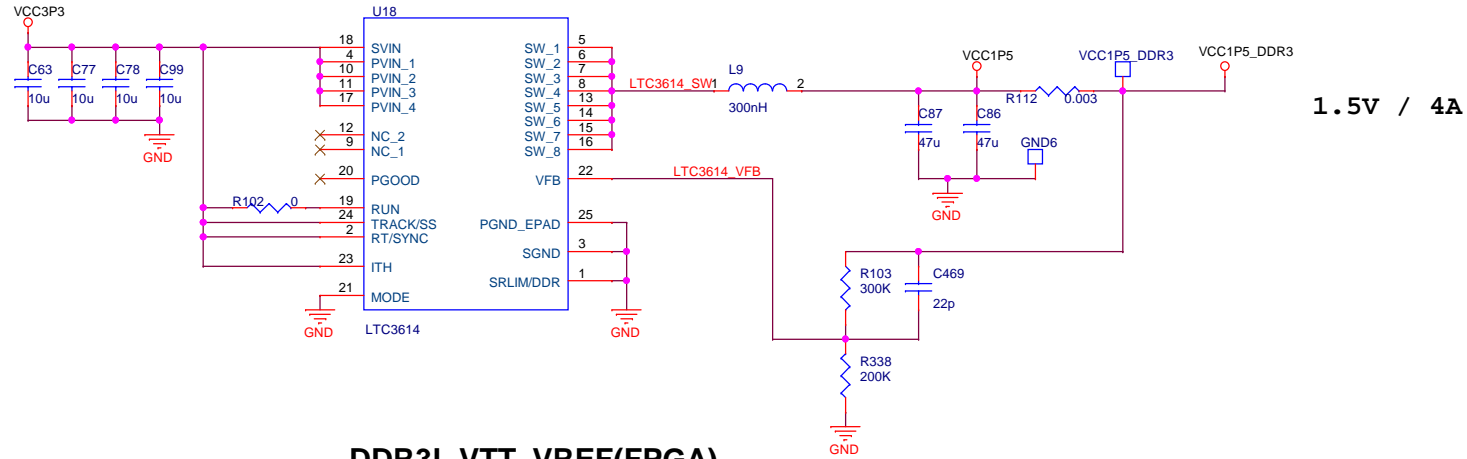


3.3V / 8A

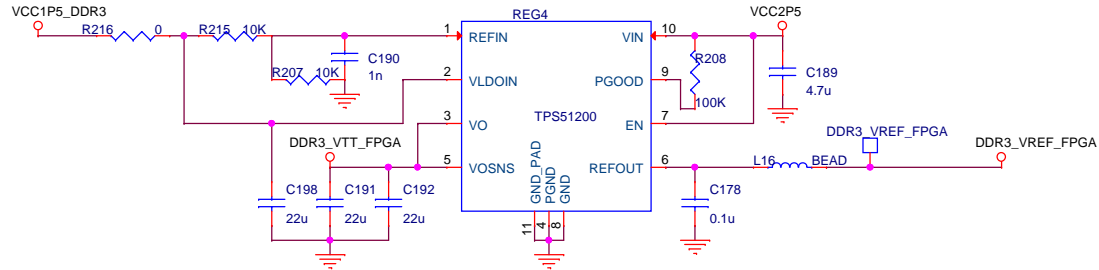


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Title		
C5S Board		
Size	Document Number	Rev
B	Power - 3.3V & 2.5V	A
Date:	Tuesday, May 07, 2013	Sheet 28 of 30

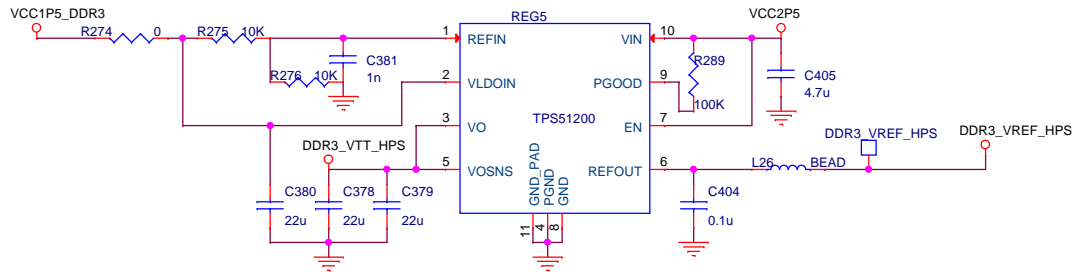
DDR3L VDD,VDDQ




DDR3L VTT, VREF(FPGA)

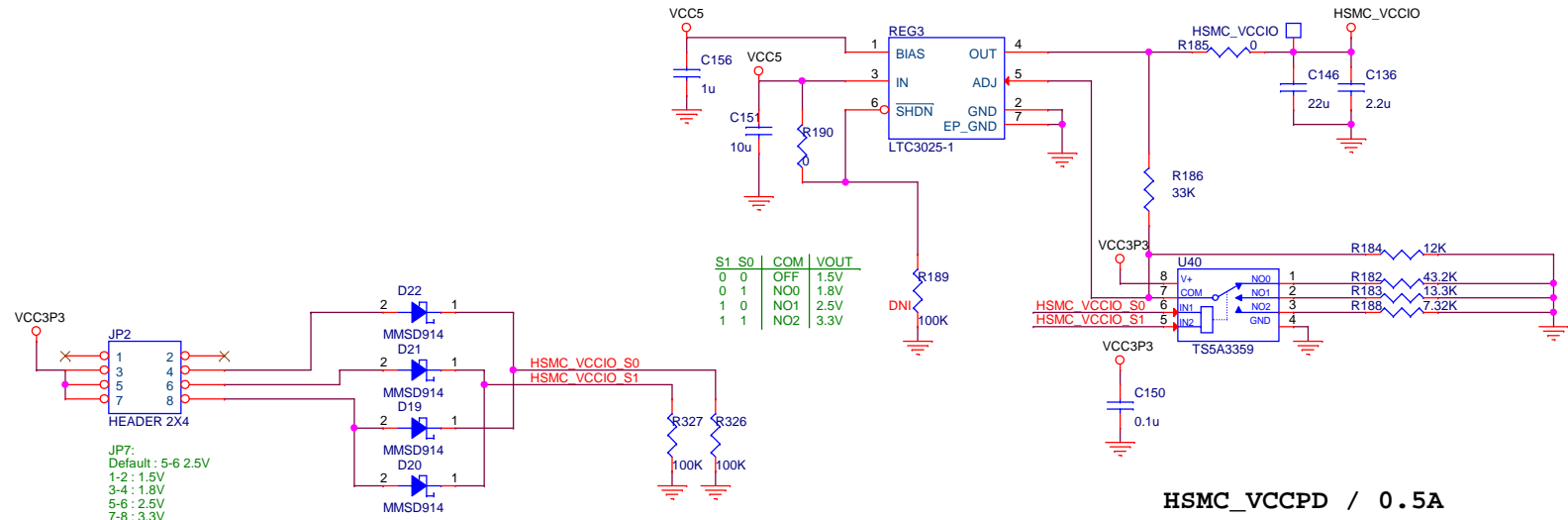


DDR3L VTT, VREF(HPS)



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Title		
C5S Board		
Size	Document Number	Rev
B	Power - 1.5V	A
Date:	Tuesday, May 07, 2013	Sheet 29 of 30

HSMC_VCCIO / 0.5A



HSMC_VCCPD / 0.5A

